AD-A143 559 NON-DESTRUCTIVE TESTING OF SEMICONDUCTORS USING SURFACE ACOUSTIC WAVE..(U) RENSSELAER POLYTECHNIC INST TROY NY DEPT OF ELECTRICAL COMPUT.. B DAVARI ET AL. 31 DEC 83 1/3

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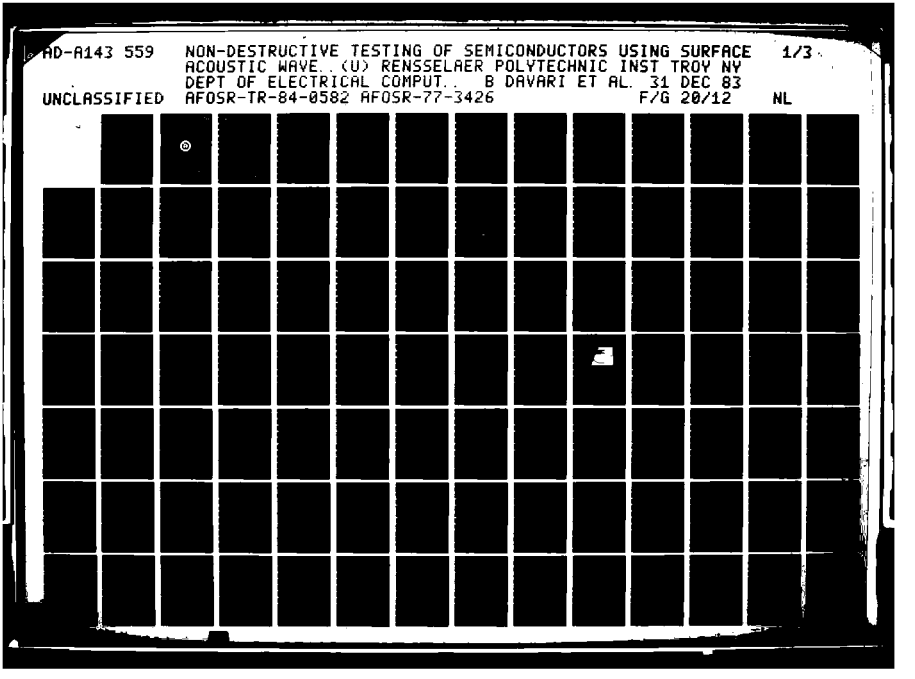

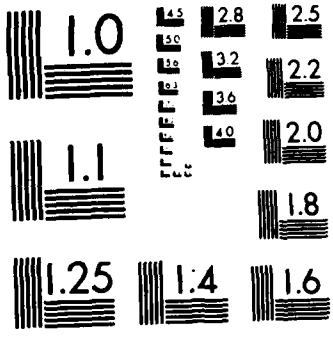

AFOSR-TR- 84-0582

(12)

NON-DESTRUCTIVE TESTING OF SEMICONDUCTORS USING SURFACE ACOUSTIC WAVE

FINAL TECHNICAL REPORT AFOSR-F-1

BY

B. DAVARI AND P. DAS

DECEMBER 31, 1983

AIR FORCE OFFICE OF SCIENTIFIC RESEARCH

GRANT NOS. AFOSR-77-3426 AND AFOSR-82-0281

ELECTRICAL, COMPUTER, AND SYSTEMS ENGINEERING DEPARTMENT
Rensselaer Polytechnic Institute
Troy, New York 12181

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered) UNCLASSIFIED

REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER AFOSR-TR- 84-0582	2. GOVT ACCESSION NO. AD-A143 539
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle) NON-DESTRUCTIVE TESTING OF SEMICONDUCTORS USING SURFACE ACOUSTIC WAVE	5. TYPE OF REPORT & PERIOD COVERED Final Technical Report
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) P. Das and B. Davari	8. CONTRACT OR GRANT NUMBER(s) AFOSR Grant No. 77-3426
9. PERFORMING ORGANIZATION NAME AND ADDRESS Electrical, Computer, & Systems Engineering Dept. Rensselaer Polytechnic Institute Troy, NY 12181	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61102F 2306/A2
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Office of Scientific Research Bolling Air Force Base Washington, D.C. 20332	12. REPORT DATE December 31, 1983
	13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report) UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Non-destructive testing, automated testing of VLSI, VIHISIC, SAW technology, SAW convolver, characterization of semiconductor interface, Si, GaAs, InP, CdS, InAs.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Properties of semiconductor surfaces and interfaces play a vital role on the electrical characteristics of the devices fabricated on semiconductor surfaces. Considering today's rapid advancements in the area of planar fabrication processes used in VIHISIC and VLSI chips, the effect of surface on device performance is of increasing importance. This report encompasses both the theoretical and experimental aspects of the research related to the characterization of silicon and compound semiconductors (such as gallium arsenide, cadmium

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sulfide) surfaces and interfaces.

The major emphasis of this report is on a new and novel surface acoustic wave (SAW) device which has been developed under this grant for use in the nondestructive determination of the electronic properties of semiconductors. The technique uses surface acoustic waves on a piezoelectric substrate. The electric field associated with the SAW interacts with free carriers of a semiconductor placed near the piezoelectric surface. The interaction generates detectable currents in the semiconductor and attenuates the SAW. By observing these effects while varying external parameters such as temperature, applied acoustic power, SAW frequency semiconductor surface irradiation and bias voltage, the desired information is obtained. The properties that can be determined by this non contact technique include the bulk and surface conductivity, generation lifetime, surface recombination velocity, the location in the energy gap of traps, surface states, and interface states, trap emission and absorption times and storage times in the depletion layer. The technique can be used to perform depth profiling of electrical properties. Because the properties are measured without any contact and the measurement is localized to a small region of the wafer, one can envision an automated equipment, using this SAW technique, where 256x256 points (for an example) on the wafer can be evaluated with respect to lifetime and surface generation velocity. The results can be shown in the form of images in pseudocolor where each color represents a certain range of the parameters.

The SAW characterization of the semiconductor could be performed at progressive stages of device fabrication thereby improving yield by identifying faulty processing steps. Thus, the implementation of the new and more conventional, alreading existing techniques (such as C-V, C-t, SEM, voltammetry, etc.) reveal the critical semiconductor surface and interface properties before and after the semiconductor has undergone a specific processing step, e.g., thermal oxidation, etching, polishing, annealing (Si) and anodic oxidation (GaAs). A brief listing of the research performed towards the application of this technique in determining different electrical properties of different semiconductors follows:

* Silicon: The nondestructive SAW technique is greatly improved by the introduction of a new delay line structure which has enabled us to vary the surface potential via a small external DC bias field (about 100 times smaller than the previous work and comparable to C-V technique) while the transverse acoustoelectric voltage (TAV) amplitude and transient time constants are measured. Parameters such as oxide charge, flatband voltage, generation lifetime and surface generation velocity are determined at different surface potentials.

* GaAs: Two beam TAV spectroscopy is applied in order to reveal the subbandgap energy level structures. In two beam spectroscopy the wavelength of one beam is fixed (bias light) while the wavelength of the second beam (secondary light) is scanned in the desired range. The presented data reveals the subbandgap interface states.

* CdS, InP, InAs (HgCd) Te: In addition to the two beam TAV spectroscopy for the subbandgap energy level studies, the following investigations are conducted regarding the above semiconductors: 1) CdS is used as the working electrode in a semiconductor liquid junction solar cell configuration. 2) Low temperature one and two beam TAV spectroscopy are performed on high resistivity Fe doped InP samples and the results demonstrate the characteristic exciton peaks and no quenching effect by bias light (as opposed to GaAs samples) which is attributed to a lower density of interface states. 3) TAV versus voltage measurements are performed on (HgCd) Te samples to reveal the surface condition at zero bias (depletion, inversion) and possibly the magnitude of the interface charges.

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PREFACE

This technical report was prepared by the Microwave Acoustics Laboratory, Electrical, Computer, and Systems Engineering Department of Rensselaer Polytechnic Institute, Troy, New York. The major support for this work came from the Air Force Office of Scientific Research Grant No. AFOSR 77-3426 (monitored by Lt. Colonel Lawson P. Mosteller, 1977-1978, Lt. Colonel C. Gardner, 1978-1980, Lt. Colonel Harry Winsor, 1980-1983). The initial support of this project also came from ONR and NSF.

This report summarizes the work related to the use of non-destructive SAW technique to evaluate and characterize electrical properties of semiconductor surface and semiconductor-insulator interface. Part of this work has already been published in the references listed in Appendix A. One patent has been obtained and another one is being filed. These are also listed in Appendix A.

Over the last six years the following people were supported by these grants:

Research Associates:

R. Webster
M. Rosenmann
P. Rademeyer

Graduate Students who finished Ph.D. Degree:

H. Estrada-Vazquez
K. Varahramyan
S. Chakravarti
B. Davari (1984)
D. Shklarsky
J. S. Moore

Graduate Students who completed Masters Degree:

B. Baxi
N. Talati
G. Hueckel
K. Varahramyan
N. Mehta
D. Barone
R. Werner
B. Davari
M. Tabib-Azar (1984)
L. Biro

Graduate Student:

N. Sanford

Undergraduate Students:

R. Coyne
E. Williams
S. Tiersten
M. Anderson
J. Rheinhold

All of the above-mentioned students contributed towards this report. However, the contributions of the following persons were indispensable. Dr. H. Estrada-Vazquez, Engineering Science, Materials and Mechanics Dept. University of North Carolina, Charlotte, Dr. K. Varahramyan, IBM Corporation, Essex Junction, VT and Mr. M. Tabib Azar.

Dr. F. M. Ayub, Bendix Corp., Columbia, MD, Dr. M. K. Roy, Bendix Corp., Columbia, MD, and Dr. S. Chakravarti, IBM Corporation, East Fishkill, NY, although not supported by this grant, contributed to this report.

Finally, we are indebted to the following people who have been co-authors of papers included in this report.

Dr. R. Bharat, Rockwell International

Dr. A. Westdorp, IBM

CHAPTER 1

INTRODUCTION

Nondestructive semiconductor characterization techniques are of ever growing interest in the rapidly advancing fields of microelectronics and semiconductor technology. One reason is their potential application in the automatic testing stations which can be incorporated in automated production lines. This is due to the monitoring capability without damaging the semiconductor which goes through a large number of fabrication steps. In this work surface acoustic wave (SAW) techniques are used as a nondestructive means to characterize the semiconductor surfaces and interfaces in conjunction with more conventional techniques such as capacitance voltage (C-V) and capacitance time (C-t) measurements. During the course of this work in the past few years the sensitivity and applicability of the SAW technique has been greatly enhanced by the introduction of a new delay line structure, a new profiling procedure and the use of two beam spectroscopy. The capabilities of the SAW technique are manifold and are listed in Tables I and II.

The main feature of the SAW technique is that the probing tool is an ac electric field which is generated at the surface of a piezoelectric material and is coupled to the semiconductor surface free carriers without any form of contact. Studies and applications of the surface acoustic waves or Rayleigh waves [1] related to the signal processing devices started in the sixties. Surface waves propagate along the free surface of a solid as opposed to bulk waves. The main distinction is that the displacement amplitude due to the passage of elastic surface waves is maximum at the free surface and decays exponentially as a function of depth in the material [2]. If the material is piezoelectric then there is

TABLE I

NDE OF SEMICONDUCTORS USING SAW

SEMICONDUCTOR PROPERTY	SAW MEASUREMENT	VARIABLES	REQUIRED ANALYSIS
1. Conductivity	TAV		Calibrate theoretical plots for each semiconductor
2. Type of majority carrier near surface	TAV		The polarity of TAV indicates carrier type: positive for n-type, negative for p-type
3. Impurity concentration depth profile	TAV	Applied bias voltage	Measure the TAV amplitude as a function of applied bias voltage using the ground path deposited on the $LiNbO_3$ surface (new structure). TAV to conductivity calibration is needed. Mathematical manipulation of the average carrier concentration depth profile should be performed to obtain the impurity concentration depth profile. Pulsed bias voltage should be used for profiling deeper than the maximum equilibrium depletion width.
4. Interface charge distribution, oxide fixed charge density and flat band voltage	TAV	Applied bias voltage	Measure the TAV amplitude versus the applied bias voltage (TAV-V) using the new structure. Compare the experimental curve to the theoretical TAV-V curve and extract the information about N_{ss} and Q_{ss}. The value of surface potential at each bias voltage can be easily obtained.
5. Generation lifetime, surface generation velocity	TAV	Applied bias voltage	TAV transient time constants are measured (τ_{eff}). τ_{eff} is approximately related to generation lifetime (τ_g) and surface generation velocity (S_g). Crude approximations of τ_g and S_g might be calculated by measuring τ_{eff} under varying applied bias voltage. Mechanisms involved in determining τ_{eff} are complicated and a comprehensive analysis of them is required for more precise evaluation of τ_g and S_g. Measurement can be adapted as a fast and automated diagnostic technique to screen the wafers which will be used in VLSI fabrication.
6. Interface state band structures (radiative states)	TAV	Two monochromatic beams	TAV amplitude is measured while the surface under study is illuminated by two monochromatic beams. Detailed energy distribution of the interface states within the band can be obtained from the two beam TAV spectral response. Exciton peaks are observed in GaAs and InP.

TABLE I (continued)

SEMICONDUCTOR PROPERTY	SAW MEASUREMENT	VARIABLES	REQUIRED ANALYSIS
7. Carrier mobility	Longitudinal acoustoelectric voltage	-	Amplitude of the longitudinal acoustoelectric voltage or current is measured. Needs two contacts to the semiconductor.
8. Annealing effectiveness (Laser or thermal)	TAV	-	Observe the change in conductivity and type of majority carrier. These indicate the extent of annealing.
9. Epitaxial layer properties	TAV or attenuation	-	SAW measurements are confined to a Debye length. Thus, the surface layer properties are obtained with little interference from the bulk.
10. Emission time constant, capture cross section	Attenuation	Scan the semiconductor with dc bias voltage while applying an additional bias pulse.	Through analysis of the effect of the pulse at each bias point obtain capture cross-section and surface state distribution as a function of energy.
11. Surface state density	Attenuation	Use dc bias voltage to scan the semiconductor surface from accumulation to depletion.	Compare scans with theoretical plots to obtain flat band voltage and surface state density.
12. Photoconductivity Response Time	Attenuation	Shine pulsed light. Use dc bias voltage to deplete or accumulate the semiconductor surface.	Measure the time constant caused by the light pulse. The effects of bulk and surface recombination can be separated by comparing data obtained under various bias conditions.
13. Carrier Generation Rate	Attenuation	Drive the semiconductor from accumulation to deep depletion by switching the dc bias voltage.	Observe the recovery of the attenuation. This time constant is the inverse of the generation rate.

TABLE II

TAV MEASUREMENT CAPABILITIES, MATERIALS AND PROCESSES

Evaluated Quantity	Measurement Procedure	Material, Processes and Comments
1. Depth profiling of the average majority carrier concentration	TAV versus applied bias voltage (TAV-V)	Phosphorous implanted, high resistivity Si samples. The measured profile is compared with the spreading resistance measurement which evaluates the impurity carrier concentration profile. The error is in the same order of magnitude as compared C-V measurements. The profiling of such parameters as mobility, generation time, ... might be possible using the new profiling procedure.
2. Evaluation of fixed oxide charge and flat band voltage	TAV-V	5" Si wafers, ρ = 11-16 Ωcm, p type, used for NMOS technology. Thermally oxidized (dry-wet-dry). Theoretical manipulation of data is more complicated than C-V. Much higher sensitivity for low carrier concentration ($N>10^{12}$ cm^{-2}) compared to C-V. Lower sensitivity for high conductivity material (not feasible for $\rho < 0.01$ Ωcm).
3. Effectiveness of the laser induced damage on the back surface as a gettering technique	TAV transient time constant measurement (τ_{eff})	5" silicon wafers, ρ = 11-16 Ωcm, p type. Half wafers have undergone the gettering process and simulated 7 or 8 step heat treatment suitable technique for comparative measurements.
4. Effect of polishing, etching and forming gas annealing	τ_{eff} and τ_{eff} versus the applied bias voltage (τ_{eff}-V)	5" silicon wafers, ρ = 11-16 Ωcm, p type. Wafers have undergone different acid etching and SiO_2 based polishing removals. Oxidized wafers are cleaned and random halves are annealed in forming gas. Good technique for comparison. Accurate measurements of lifetime needs a thorough investigation.

an electric field associated with the surface acoustic wave which extends above the material surface. The basic mechanism, exploited in the diverse field of signal processing using SAW devices [9,10], is the interaction of these electric fields with metal electrodes placed on the surface [3]. The complicated configurations of the metal electrodes which are utilized today in SAW devices [11-17] are different combinations of the interdigital transducer (IDT) configuration [4].

The interaction between the electric field accompanying SAW and semiconductor electrodes are of special importance [18-32]. The basic experimental configuration used in the SAW-semiconductor testing is illustrated in fig. 1.1. The central feature is a SAW delay line which consists of a piezoelectric substrate with a highly polished surface on which IDT's are formed by photolithographic techniques. In this work the piezoelectric material is a y cut, z propagating $LiNbO_3$ substrate. The IDT's are thin film Aℓ fingers (1 μm) alternately connected to bus pads as shown in fig. 1.1b. An RF voltage applied to the transducer creates an alternating electric field which penetrates the substrate causing stress via the piezoelectric effect [4]. If the periodicity of the transducer is such that the alternating electric field reinforces the stress waves as they travel beneath adjacent fingers of the transducer, then surface acoustic waves are generated. This condition is met if adjacent fingers, each 1/4 wavelength wide are separated by 1/4 wavelength for the particular piezoelectric (particular SAW velocity) and frequency under consideration. By increasing the number of fingers of IDT the coupling efficiency of the transducers increases, while the frequency of bandwidth decreases [5,6]. The SAW propagates along the surface of the substrate creating stress variations which decay exponentially with depth

into the substrate. Because of the piezoelectric effect, the propagating stress waves are coupled to propagating electric field which has components both perpendicular and parallel to the surface of $LiNbO_3$. As will be shown later the perpendicular component is the probing field, utilized in this work. The electric field exists both inside and outside the piezoelectric and decays exponentially with distance from the surface. The decay constant in the free space above the delay line is the SAW wavelength. As a result, when the SAW passes under an identical IDT, after some delay, an RF voltage is generated across the transducer. Thus the structure can be used as a delay line and is called as such [8]. Typical frequency range for SAW devices is between 30 MHz to a few GHz. In the experiments reported here, 55 or 110 MHz SAW delay lines are used. On y-z $LiNbO_3$ the SAW velocity is about 348800 cm/sec. Therefore the SAW wavelength is approximately 32 μm and the delay per unit length is about 2.9 μsec/cm. Both linear and nonlinear interactions of the RF electric field with the semiconductor near surface free carriers are of interest. The earlier works treat the interaction mechanism itself as well as its applications for such devices as SAW amplifiers and convolvers [20,19,22]. Evaluation of the semiconductor electrical properties using SAW started with measurements of carrier mobilities in CdS as deposited on quartz substrate [18] and silicon accumulation layer [31]. Transient response of Ge samples were studied under pulsed bias field [38]. Different mechanical configurations are realized using semiconductor interaction medium. They include: 1) The separated medium structure, where a slab of semiconductor is placed at close proximity above the piezoelectric substrate with the possible presence of an air gap through which the coupling between the electric field and the semiconductor free carriers takes place (e.g., Si on $LiNbO_3$ [34]). 2) The

combined medium where a slab of piezoelectric semiconductor such as CdS or GaAs serves both as the delay line and interaction medium [36]. In the present work the separated medium structure is chosen for semicondcutor characterization due to its versatility and nondestructive nature. When the probing electric field reaches under the semiconductor surface (fig. 1.1), the nonlinear interaction with the free carriers of the semiconductor develops a voltage across the semiconductor. The dc transverse component of this voltage which is called the transverse acoustoelectric voltage (TAV) is the monitored signal throughout the experiments reported here. Other effects of the nonlinear interaction are: the reduction of the SAW velocity [20,29], the attenuation of the output signal (propagation loss) [18], the generation of convolution voltage across the semiconductor and parametric amplification if both transducers are used as inputs [22-28].

The source of nonlinear interaction can be qualitatively explained as follows. The time varying electric field associated with SAW modulates the free carrier concentration within the interaction depth according to the Poisson's equation. The simultaneous presence of the free carriers and electric field generates an acoustoelectric current which is proportional to their multiplication. Carrier concentration and electric field both contain time varying terms, thus their multiplication generates current with dc and multiples of the center frequency components which is characteristic of nonlinear interaction. For open circuit condition the total steady state current within the semiconductor is zero leading to the generation of the transverse electric field. Integration of the induced electric field across the semiconductor yields the transverse acoustoelectric voltage (TAV). It is important to note that the penetration depth of the probing electric field is on the order of the semiconductor extrinsic Debye

length or the acoustic wavelength whichever is shorter.

Nondestructive measurements of semiconductor surface properties began by utilizing the above nonlinear interaction [39,42]. In the present work the TAV signal is exclusively used for the characterization of semiconductor surfaces and interfaces. TAV amplitude is dependent on the conductivity difference between electrons and holes in the interaction region (with a thickness of about an extrinsic Debye length). A theoretical background regarding the calculation of the TAV amplitude as a function of carrier concentration is presented in Chapter 2. Semiconductor characterization is performed by varying the free carrier concentration within the interaction region while monitoring the TAV signal [42,71]. Carrier concentration can be modulated by photons, heating or cooling and applied bias voltage across the semiconductor (field effect). TAV signal can be monitored by placing a metal plate above the semiconductor and another one below the $LiNbO_3$ substrate (fig. 1.1). To monitor the dc TAV signal through the possible insulators, the RF voltage and thus the probing electric field are pulsed. TAV is capacitively coupled to the metal plates, so the presence or absence of insulator layer on the semiconductor surface is immaterial. For spectroscopic measurements, the configuration of figure 1.1 is used [45-47] where the ground path is an Al plate evaporated underneath the $LiNbO_3$ and one or two monochromatic incident beams are shone on the semiconductor surface through a small window. This structure is only sufficient for spectroscopic measurements where the modulation of the surface potential by an external bias voltage is not needed. On the contrary, if the surface potential has to be modulated, a very large voltage in excess of 1000 volts is needed to sustain the voltage drop across the thick $LiNbO_3$ structure ($\simeq$ 3 mm) [43,48,49]. To overcome this

problem a new delay line structure is devised which provides an alternative ground path for the TAV signal [50].

The new structure eliminates the voltage drop across the $LiNbO_3$ and thus reduces the necessary applied bias range (in field effect measurements) to 10 volts [50] as compared to 1000 volts needed previously [49]. The combination of nondestructive nature of the TAV measurement and the ability to readily modulate the surface potential leads to a powerful measurement technique. The class of nondestructive measurements under applied bias voltage is discussed in Chapter 3 which includes: 1) a detailed discussion of the new delay line structure, 2) the development of the theoretical foundation needed to utilize the potential of the TAV versus voltage (TAV-V) measurements. The subjects presented under this heading are: 2-1) A new profiling procedure, applicable to the measurements where the free carrier concentration is the primary measured quantity [51,52]. The technique is applied to (TAV-V) measurements since the TAV amplitude is a function of the free carrier concentration [50]. The distinct difference between the pulsed capacitance-voltage (C-V) measurements [53-58] and the proposed procedure is that in the former measurable physical quantity is the depletion layer width which is modulated by an external field. In the latter, the carrier concentration as a function of bias field is monitored and the depletion layer width is then calculated. The possibility of depth profiling of such properties as interface states energy levels and carrier lifetime are discussed. 3) Nondestructive characterization of the semiconductor/insulator interface by monitoring such parameters as insulator fixed charges, interface states density, and flat band voltage is demonstrated [50]. The basis of the measurement is the comparison between the theoretical TAV-V curve

(for a specific semiconductor, insulator dielectric constant and thickness) and the experimental one. Deviations of the experimental TAV-V curve from the calculated values are attributed to interface states and insulator charges. This method might be adopted as an alternative to C-V measurements [58,59]. An estimate of the carriers generation lifetime (τ_g) and surface generation velocity (S_g) can be obtained by measuring the TAV transient time constants (τ_{eff}) [60,61]. These parameters which are indications of the defect density and surface conditions are determined by capture and emission rate of carriers and density of deep traps within the semiconductor band gap. Trap properties are conventionally studied by transient capacitance measurements regarding the buildup of the inversion layer in MIS structures are also used to determine τ_g and S_g [67-70]. The separation of τ_g and S_g in this work is done by the application of a depleting bias field across the semiconductor while monitoring τ_{eff} (τ_{eff} versus voltage measurements). This technique can be adopted as a fast and automated diagnostic technique to screen the wafers which are used in VLSI fabrication. Theoretical treatments in this chapter are presented for the first time and they are not complete in some parts (as will be shown in detail in the corresponding sections), but nevertheless they present a viable foundation for the future work in the related area.

The applications of the theoretical analysis in Chapter 3 are demonstrated by the experimental results presented in chapter 4. In this chapter the TAV measurements under applied bias voltage are mainly used to characterize the effect of different fabrication processes on the silicon wafers. The processes used in VLSI fabrication such as ion implantation, thermal oxidation, laser induced damage gettering, polishing,

etching and annealing are investigated nondestructively by monitoring such parameters as free carrier concentration depth profiles, oxide charge, generation lifetime and surface generation velocity. One advantage of the TAV technique is that there is no need to fabricate a contact to semiconductor surfaces which is to be studied. Also the measurement sensitivity for high resistivity samples is much higher than C-V or Hall measurements (e.g., carrier concentration on the order of 10^{12} cm^{-3} is detectable in Si). The fundamental disadvantage of the TAV is the low sensitivity for low resistivity samples ($\rho \leq 0.012$ cm).

In the following chapters the double beam TAV spectroscopy along with other techniques such as C-V are used to investigate the property of semiconductor surfaces and interfaces [47,71,72], where a bias light with a fixed wave length illuminates the sample while the wavelength of another incident beam (secondary light) is scanned in the desired range. The main problem of the devices made with GaAs MOS technology using native oxide is the anomalous behavior under dc and low frequency operation, and the long term stability of the device. This behavior is due to the high density of interface states present at the GaAs/oxide interface. An extensive effort has been carried out for the better understanding of the complicated nature of the GaAs/oxide interface [78,82] and the anodic oxidation mechanism [73-77]. Investigation of GaAs samples and the effect of different anodic oxidation schemes on the GaAs/oxide interface and oxide bulk properties are presented in Chapter 6. The subjects include the following. 1) Two beam TAV spectroscopic study of interface states energy levels of bare and anodically oxidized [73] (wet oxidation under constant current density regime) semi-insulating GaAs (Cr doped) samples. The results indicate the presence of a high density acceptor level at about

1 eV above the valence band for unoxidized GaAs [47]. Anodic oxidation increases the density of this acceptor level and also another donor level at about 1.3 eV below the conduction band becomes detectable after oxidation. Higher oxidation current density results in the higher density of interface states. 2) The investigation is extended to low resistivity p and n type GaAs samples using C-V measurements [83,84]. The results show that the higher current density of oxidation does increase the interface states density but it produces an oxide with superior bulk properties such as low injection type hysteresis and higher breakdown field. An optimum current density waveform has also been devised which starts at low current to produce a lower interface states density in the oxide nucleation phase, followed by a high current density in the continuous oxide growth phase in order to produce a high quality oxide bulk. 3) Low temperature two beam TAV spectroscopy of GaAs leads to the detection of the characteristic exciton peaks [85-89] and the quenching of the peaks [90-94] is observed upon shining a 1 eV bias light. The quenching effect is attributed to the increase in the hole density by electron transition from the valence band to the high density acceptor level, causing a higher recombination rate and therefore destroying the exciton states [85]. This effect is not observed in InP samples due to lower density of interface states [71]. In chapter 7 the studies of CdS samples, which are used as the working electrode in the CdS/$K_4[Fe(CN)_6]$/metal liquid junction solar cell configuration [97-101] are presented [45,95,96]. Two beam spectroscopy of CdS after it has been used under short circuit current condition reveals two acceptor levels located at 0.8 and 1.3 eV above the valence band. These states are partially attributed to the nonstochiometric sulfur deposition at the CdS surface by photo-anodic dissolution of CdS

into solid sulfur and Cd^{2+} ions. These states influence the competition between the redox charge transfer and the photo-anodic dissolution process which is studied by cyclic voltammetry [102-104]. The factors affecting the cell efficiency such as the production of a thin insulating layer through which the photo current passes by tunneling and the effect of counter electrode material (e.g., Au or Pt) are discussed. At the end a brief discussion of the TAV measurements as applied to (Hg Cd)Te which is being used in focal plane array IR detectors is presented [105].

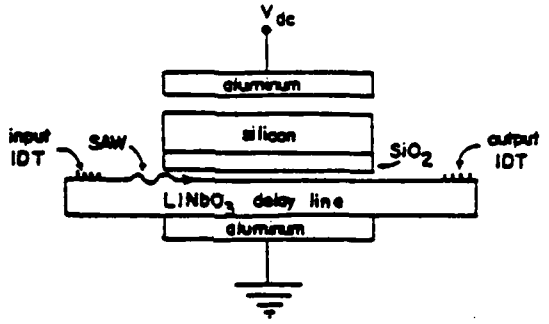

Fig. 1(a). Schematic representation of the silicon on $LiNbO_3$ separate media convolver structure.

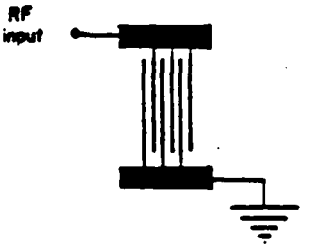

Fig. 1(b). Representation of the interdigital transducer used to generate surface acoustic waves.

Figure 1.1

CHAPTER 2

DEVELOPMENT OF TRANSVERSE ACOUSTOELECTRIC VOLTAGE (THEORETICAL BACKGROUND)

In this chapter the theoretical calculations, leading to the formulation of the Transverse Acoustoelectric Voltage (TAV) as a function of the carrier concentration are presented. SAW semiconductor interaction has been studied earlier in relation to SAW amplifiers and convolvers [19-28]. TAV is generated as a result of nonlinear interaction between the rf electric field accompanying SAW and the semiconductor free carriers. The general configuration of the problem is shown in figure 2.1. SAW is propagating on the piezoelectric ($LiNbO_3$) surface in the z direction with the accompanied probing electric field extending in the y direction and the semiconductor is placed above the $LiNbO_3$. The distance between the semiconductor and $LiNbO_3$ is assumed to be zero which is a reasonable assumption if this distance is much smaller than the SAW wavelength, λ_{SAW} (λ_{SAW} = 32 μm or 64 μm for SAW frequency of 110 MHz or 55 MHz respectively). The time varying probing electric field modulates the free carrier concentration as well as applying a force to them. Therefore an acoustoelectric current with nonzero steady state value is developed [23]. If the measurement is voltage sensitive, then the total steady state current in the y direction (figure 2.1) is zero. Thus a steady state electric field is set in the y direction, the integration of which across the semiconductor (from y=0 to y=t_s = semiconductor thickness) yields the transverse

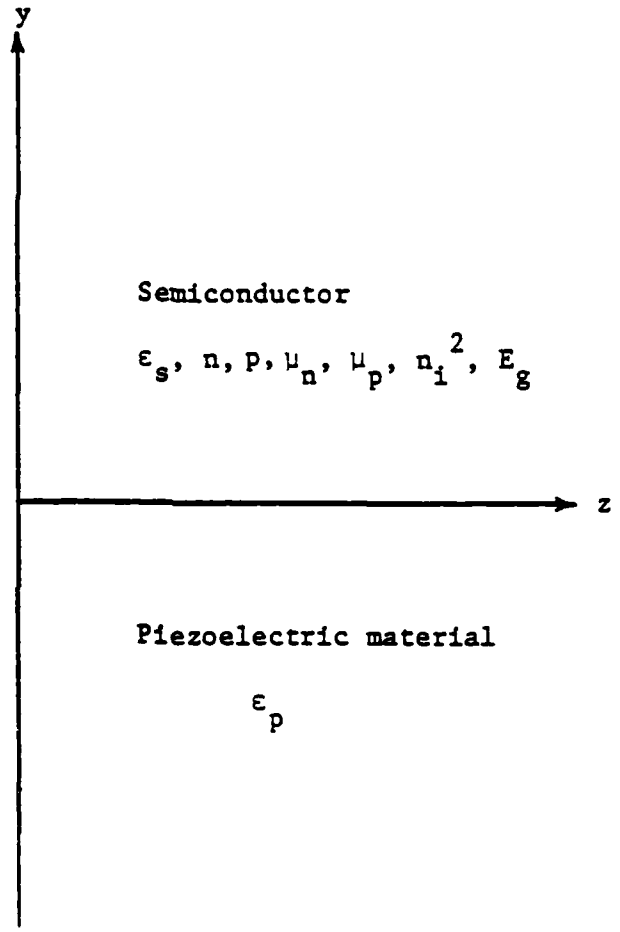

Figure 2.1 The spatial configuration of the semiconductor/piezoelectric, used in SAW measurements

acoustoelectric voltage (TAV). The TAV signal is detected across the semiconductor via a contact to the semiconductor back surface, and the surface under study provides the ground terminal as will be discussed in more detail in the next chapter. The interaction strength between the probing electric field and free carriers is a function of the free carrier concentration. At very low and high densities the interaction is weaker which is reflected in the drop of the TAV amplitude at these concentrations. The reason is that at very low concentrations there are not enough carriers to interact with and at high concentrations the electric field is effectively shielded by the free carriers (e.g., low and high carrier concentration values for Si are in the range of 10^{12} and 10^{18} cm^{-3}). The penetration depth of the probing field in the semiconductor is on the order of the extrinsic Debye length. The net effect of the rf field in extrinsic semiconductors is to establish a weak depletion in the interaction region. The reason is that at the half cycles corresponding to the accumulation of the semiconductor, the Debye length decreases, and it increases for the half cycles associated with depletion. Thus in average a weak depletion is developed which can be compared to the depletion established by applying a small DC bias voltage across the semiconductor. If the extrinsic Debye length of the semiconductor is very large, then the penetration depth of the probing field is determined by the acoustic wavelength. The polarity of the TAV signal is positive for net electron conductivity and negative for hole conductivity, if the ground voltage is assumed at

the surface facing the $LiNbO_3$ (surface under study). This effect which is very useful in determining the type of surface conductivity is due to the fact that a positive voltage at the back surface is needed (equivalent to substrate biasing in MOS structure) to deplete the n type semiconductor (on the device side) and it should be negative for p type. The theoretical calculation of the TAV amplitude as a function of carrier density is presented in the next section.

2.1 Theoretical Evaluation of the TAV Amplitude

The flow chart of the TAV calculation procedure is shown in figure 2.2. An electric potential which is propagating in the z direction with angular frequency (ω) and wavelength (λ) is assumed in the form $\phi = \phi(y)e^{j(\omega t - kz)}$ [29], where $\phi(y)$ is the amplitude of the electric potential in the y direction. Inside the semiconductor ($y > 0$) a fourth order differential equation for $\phi(y)$ can be established using continuity, current and Poisson's equations. The solution of this equation is in the form $A_1e^{-ky} + A_2e^{-\gamma ky}$ if the semiconductor thickness (t_s) is much larger than the acoustic wavelength. Using the appropriate boundary conditions for ac current and electric potential at the semiconductor and $LiNbO_3$ surfaces [37] the values of γ, A_1 and A_2 can be determined, leading to the solution for ϕ. Once ϕ is known, then the ac electric field in the y direction (E(y)) and excess carrier concentrations (n_1, p_1) can be formulated. The nonlinear acoustoelectric

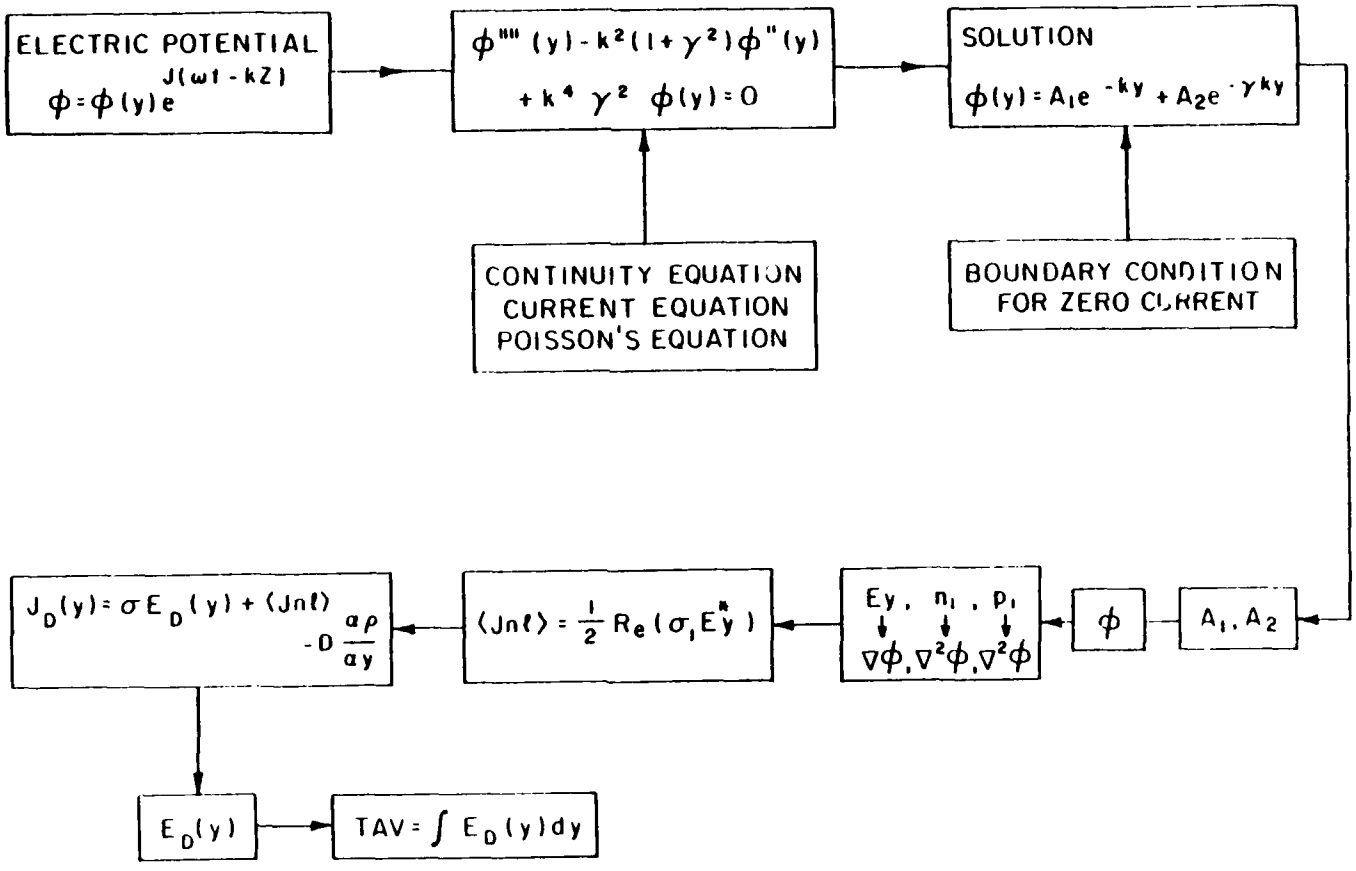

Figure 2.2 Block diagram of the TAV-n calculation procedure.

current density ($J_{n\ell}$) is obtained from E(y), n_1 and p_1. The total steady state current density ($J_d(y)$) is then considered which contains the contributions of the drift, diffusion and dc term of the nonlinear current. By using proper boundary conditions regarding the steady state current densities, the steady state transverse electric field (y direction) is found. The integration of this electric field across the semiconductor yields the TAV. The mathematical formulation is as follows.

The rf electric potential can be demonstrated as:

$$\phi(y,z,t) = \phi(y)\, e^{j(\omega t - kz)} \tag{2.1}$$

where ω = SAW angular frequency

$k = \frac{\omega}{v_s}$ = wave number

v_s = SAW velocity = 348800 cm/sec in y cut z propagating $LiNbO_3$.

From this point on, all the time and space varying quantities will be presented in the $F(y)\, e^{j(\omega t - kz)}$ form. For parameters with nonzero equilibrium values the subscript 1 is used for the perturbed quantities, e.g., the modulated excess electron and hole concentrations are denoted by n_1 and P_1. The general current, continuity and Poisson's equations are:

$$J = \sigma E - D\nabla\rho \tag{2.2}$$

$$\nabla . J = \frac{-\partial\rho}{\partial t} \tag{2.3}$$

$$\nabla^2 \phi = - \frac{\rho}{\varepsilon_s} \tag{2.4}$$

where J = current density

σ = electrical conductivity

D = free carrier diffusion constant

ρ = charge density

ε_s = semiconductor permittivity

The small signal equations for time varying quantities at fundamental frequency are obtained by subtracting the equilibrium terms from the general equations and neglecting the second order terms. The current equations for electrons are:

$$J_n(y) = q\mu_n \, n \, E(y) + q \, D_n \frac{dn_1}{dy} \tag{2.5}$$

$$J_n(z) = q\mu_n \, n \, E(z) - jk \, q \, D_n \, n_1 \tag{2.6}$$

For holes:

$$J_p(y) = q\mu_p \, P \, E(y) - q \, D_p \frac{dP_1}{dy} \tag{2.7}$$

$$J_p(z) = q\mu_p \, P \, E(z) + jk \, q \, D_p \, P_1 \tag{2.8}$$

The continuity equations are:

$$j\omega q \, n_1 = - jk \, J_n(z) + \frac{\partial J_n(y)}{\partial y} \tag{2.9}$$

$$j\omega q \, P_1 = jk \, J_p(z) - \frac{\partial J_p(y)}{\partial y} \tag{2.10}$$

where q = electronic charge = 1.6×10^{-19} coulomb

μ_n, μ_p = electron and hole mobilities respectively

D_n, D_p = electron and hole diffusion constants

n, p = time and space independent electron and hole concentrations

n_1, p_1 = excess electron and hole concentrations.

It should be mentioned that in the continuity equations the generation and recombination of free carriers at SAW frequency are ignored. The bulk mobility is used in the above equations. The Poisson's equations are (no variation in x direction):

$$\nabla^2\phi = \frac{d^2\phi}{dy^2} - k^2\phi = -\frac{q}{\varepsilon_s}(P_1 - n_1) \tag{2.11}$$

and $$E = -\nabla\phi \tag{2.12}$$

Using equations (2.1), (2.5-2.12) the following equation for $\phi(y)$ is found:

$$\frac{d^4\phi(y)}{dy^4} - k^2(1+\gamma^2)\frac{d^2\phi(y)}{dy^2} + k^4\gamma^2\phi(y) = 0 \tag{2.13}$$

where γ can be obtained from the following equation:

$$(\gamma^2 - 1)^2\left[\frac{\omega_{cp}}{D_p(\gamma^2 - k^2) - j\omega} + \frac{\omega_{cn}}{D_n(\gamma^2 - k^2) - j\omega} - 1\right] = 0 \tag{2.14}$$

The roots of the above equation are:

$$\gamma_1^2 = 1 \tag{2.15}$$

$$\gamma_2^2 = 1 + \frac{\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp}}{\omega^2} + j\,\frac{\omega_{cn}\,\omega_{Dn}^2 + \omega_{cp}\,\omega_{Dp}^2}{\omega(\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp})} \tag{2.16}$$

$$\gamma_3^2 = 1 + j \frac{\omega_{cn}\,\omega_{Dn}\,\omega_{Dp} + \omega_{cp}\,\omega_{Dp}\,\omega_{Dn}}{\omega(\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{dp})} \tag{2.17}$$

In the above equations

ω_{cn} = dielectric relaxation frequency for electrons = $\frac{q\,\mu_n\,n}{\varepsilon_s}$

$\omega_{cp} = \frac{\sigma_p}{\varepsilon_s}$

ω_{Dn} = electrons diffusion frequency = $\frac{\nu_s^2}{D_n}$

$\omega_{Dp} = \frac{\nu_s^2}{D_p}$

If $\omega > \omega_{Dn}$, ω_{Dp}, then γ_2 can be reduced to

$$\gamma_2^2 = 1 + \frac{\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp}}{\omega^2} \tag{2.18}$$

and γ_3 is close to unity.

The solution of equation (2.13) can be written in the following form

$$\phi(y) = A_1\, e^{-ky} + A_2\, e^{-\gamma ky} + A_3\, e^{ky} + A_4\, e^{\gamma ky} \tag{2.19}$$

If the semiconductor thickness is much larger than the SAW wavelength, then the coefficients A_3 and A_4 should be zero. Therefore:

$$\phi(y) = A_1\, e^{-ky} + A_2\, e^{-\gamma ky} \tag{2.20}$$

By using the boundary condition for ac current density at y = 0 and neglecting the surface recombination velocity, the following relationship is obtained between A_1 and A_2.

$$\frac{A_1}{A_2} = j\omega R \tag{2.21}$$

where $$R = \frac{\omega_{cn}\,\omega_{Dn}^{2} + \omega_{cp}\,\omega_{Dp}^{2}}{(\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp})^{2}}\,\gamma \tag{2.22}$$

γ in equations (2.20), and (2.22) is equal to γ_2 in equation (2.18), even though equation (2.16) is used in deriving equation (2.21). The reason is that the real part of γ_2 (equation (2.16)) cancels out in the ac current density formula (which is used to obtain (2.21)) and the imaginary part is not negligible. But in the following equations only the real part of γ as shown in equation (2.18) might be used.

The total steady state dc current density in the y direction is: (dc terms are nenoted by the subscript d)

$$J_d(y) = \sigma\, E_d(y) + \langle J_{n\ell} \rangle - D\,\frac{\partial \rho_d}{\partial y} \tag{2.23}$$

The time average of the nonlinear acoustoelectric current ($J_{n\ell}$) can be written as follows:

$$\langle J_{n\ell} \rangle = \frac{1}{2}\,\mathrm{Re}\,(\sigma_1\, E^{*}(y)) \tag{2.24}$$

where $\sigma_1 = q(\mu_n\, n_1 + \mu_p\, P_1)$.

Excess electron and hole concentrations (n_1, P_1) can be obtained by solving Poisson's and continuity equations:

$$n_1 = \frac{\varepsilon_s}{q}\,\nabla^2\,\phi\,\frac{\omega_{cn}\,\omega_{Dn}}{\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp}} \tag{2.25}$$

$$P_1 = -\frac{\varepsilon_s}{q}\,\nabla^2\,\phi\,\frac{\omega_{cp}\,\omega_{Dp}}{\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp}} \tag{2.26}$$

Using equations (2.11), (2.18), (2.20), (2.25) and (2.26) leads to:

$$n_1 = \frac{\varepsilon_s}{q} A_2 k^2(\gamma^2 - 1) \frac{\omega_{cn}\,\omega_{Dn}}{\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp}} e^{-\gamma k y}$$

$$= \frac{\varepsilon_s}{q} A_2 k^2 \left(\frac{\omega_{cn}\,\omega_{Dn}}{\omega^2}\right) e^{-\gamma k y} \qquad (2.27)$$

$$P_1 = -\frac{\varepsilon_s}{q} A_2 k^2(\gamma^2 - 1) \frac{\omega_{cp}\,\omega_{Dp}}{\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp}} e^{-\gamma k y}$$

$$= -\frac{\varepsilon_s}{q} A_2 k^2 \left(\frac{\omega_{cp}\,\omega_{Dp}}{\omega^2}\right) e^{-\gamma k y} \qquad (2.28)$$

The amplitude of the ac electric field in the y direction is:

$$E(y) = -\frac{d\phi(y)}{dy} = k A_1 e^{-ky} + \gamma k A_2 e^{-\gamma k y} \qquad (2.29)$$

$\langle J_{n\ell} \rangle$ can be obtained using equations (2.21), (2.24), (2.27), (2.28) and (2.29).

$$\langle J_{n\ell} \rangle = \frac{\varepsilon_s k^3 \gamma}{2} (A_2\, A_2^*) \left(\frac{\mu_n\,\omega_{cn}\,\omega_{Dn} - \mu_p\,\omega_{cp}\,\omega_{Dp}}{\omega^2}\right) e^{-2\gamma k y} \qquad (2.30)$$

In order to find $A_2\, A_2^*$, the electric potential at y=0 is considered

$$\phi(0) = A_1 + A_2 \qquad (2.31)$$

Using equations (2.21) and (2.31) we have:

$$A_2\, A_2^* = \frac{|\phi(0)|^2}{1 + \omega^2 R^2} \qquad (2.32)$$

$E_d(y)$ can now be obtained by using equations (2.23), (2.30), and (2.32). By the application of boundary conditions given by

$J_d(0) = J_d(\infty) = 0$ and continuity equation which dictates $\frac{\partial J_d(y)}{\partial y} = 0$, the transverse acoustoelectric voltage (TAV) can be obtained:

$$TAV = \int_0^\infty E_d(y)\, dy \tag{2.33}$$

In calculating TAV it can be assumed that γk which is the effective decay constant of the electric potential inside the semiconductor is on the order of the inverse of the extrinsic Debye length $(L_D)^{-1}$. To demonstrate this approximation an n type extrinsic semiconductor ($n >> p$) can be considered.

$$L_D = \left(\frac{\varepsilon_s K_B T}{q^2 (n + p)}\right)^{1/2} \simeq \left(\frac{\varepsilon_s K_B T}{q^2 n}\right)^{1/2} \tag{2.34}$$

where K_B = Boltzman's constant

T = absolute temperature.

From equation (2.18):

$$\gamma^2 = 1 + \frac{\omega_{cn}\,\omega_{Dn} + \omega_{cp}\,\omega_{Dp}}{\omega^2},$$

if $\omega_{cn}\,\omega_{Dn} >> \omega^2$ and $\omega_{cn} >> \omega_{cp}$ then $\gamma^2 \simeq \frac{\omega_{cn}}{\omega^2}$.

Thus:

$$\gamma k = \left(\frac{\omega_{cn}}{2}\right)^{1/2} \times \frac{\omega}{v_s} = \left(\frac{\sigma_n}{\varepsilon_s v_s}\right)^{1/2} = \left(\frac{q^2 n}{\varepsilon_s K_B T}\right)^{1/2}$$

and: $\gamma k \simeq (L_D)^{-1}$.

By using equation (2.33) TAV can be calculated as follows:

$$TAV = \frac{k^2}{12(\omega_{cn}+\omega_{cp})}\left(\frac{\mu_n\,\omega_{cn}\,\omega_{Dn} - \mu_p\,\omega_{cp}\,\omega_{Dp}}{\omega^2}\right)\left(\frac{|\phi(0)|^2}{1+\omega^2\,R^2}\right) \qquad (2.35)$$

Following reference [37], the electric potential at the surface of the $LiNbO_3$ can be written as:

$$\phi(0) = \left(\frac{4\alpha\,S_z}{K\,Re(1/Z_A^*)}\right)^{1/2} \qquad (2.36)$$

where

S_z = power flux per unit length

α = propagation loss

K = electromechanical coupling coefficient

Z_A = surface impedance of the piezoelectric substrate.

Both Z_A and α are affected by the semiconductor medium, adjacent to the piezoelectric surface. The equations for Z_A and α are:

$$Z_A = \frac{j}{\nu_s\,\varepsilon_s} \times \frac{1+j\omega R}{\gamma + j\omega R}\,, \quad R \text{ defined in (2.22)} \qquad (2.37)$$

and

$$\alpha = -\frac{K^2}{2}\,k\;Im\,\frac{\varepsilon_p\,\nu_s\,Z_A}{\varepsilon_p\,\nu_s\,Z_A + j} \qquad (2.38)$$

where ε_p is the permittivity of the piezoelectric material.

Using equations (2.22), (2.32), and (2.36)-(2.38) we have:

$$|\phi(0)|^2 = \frac{2\,K^2\,S_z\,\varepsilon_p(1+\omega^2\,R^2)}{\varepsilon_s^{\,2}\,\nu_s\,k\left[\omega^2\,R^2\left(1+\frac{\varepsilon_p}{\varepsilon_s}\right)^2 + \left(\gamma+\frac{\varepsilon_p}{\varepsilon_s}\right)^2\right]} \qquad (2.39)$$

By inserting $|\phi(0)|^2$ from equation (2.39) in equation (2.35) TAV can be written as

$$TAV = V_o \left(\frac{n\mu_n - p\mu_p}{n\mu_n + p\mu_p} \right) \frac{1}{\omega^2 R^2 \left(1 + \frac{\varepsilon_p}{\varepsilon_s}\right)^2 + \left(\gamma + \frac{\varepsilon_p}{\varepsilon_s}\right)^2} \qquad (2.40)$$

where $$V_o = \frac{K^2 S_z \varepsilon_p q}{6 \varepsilon_s^2 \omega K_B T} \qquad (2.41)$$

As shown in equation (2.41) the constant V_o is a function of the electromechanical coupling coefficient, acoustic power, SAW frequency and temperature. The TAV dependency on the carrier concentration (TAV-n) for Si and GaAs is calculated using equation (2.40) and the plots are shown in figures 2.3 and 2.4 respectively. Figures 2.3a,b include two plots (each), the solid curve is the (TAV-n) as calculated from equation (2.40). The dashed curve is the (TAV-n) plot from the equation presented in reference [42] where a ωR term appears in the numerator due to miscalculation. Figure 2.3a is for the SAW frequency of 110 MHz and 2.3b for 55 MHz. Additional theoretical treatments considering nonzero distance between the semiconductor and the delay line [43], and including the imaginary term of γ (equation (2.16)) and the diffusion term (equation (2.23)) while using the one carrier (electrons or holes) interaction approximation [44] were presented recently.

The important features of the (TAV-n) plots that were qualitatively discussed in the beginning of this chapter can now be observed in figures 2.3 and 2.4. These features are: 1) n type

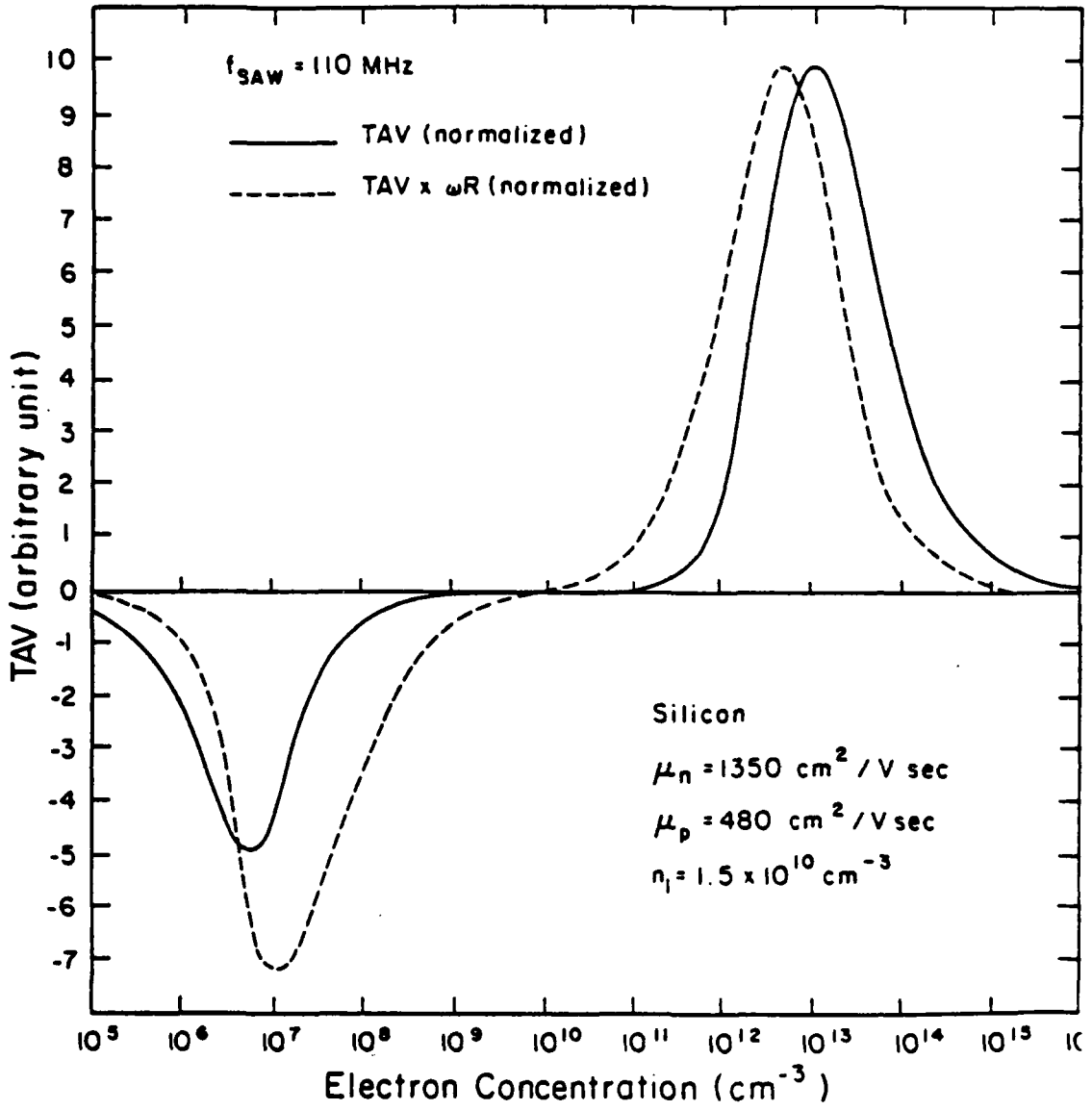

Figure 2.3a Transverse acoustoelectric voltage amplitude as a function of carrier concentration in silicon, SAW frequency = 110 MHz.

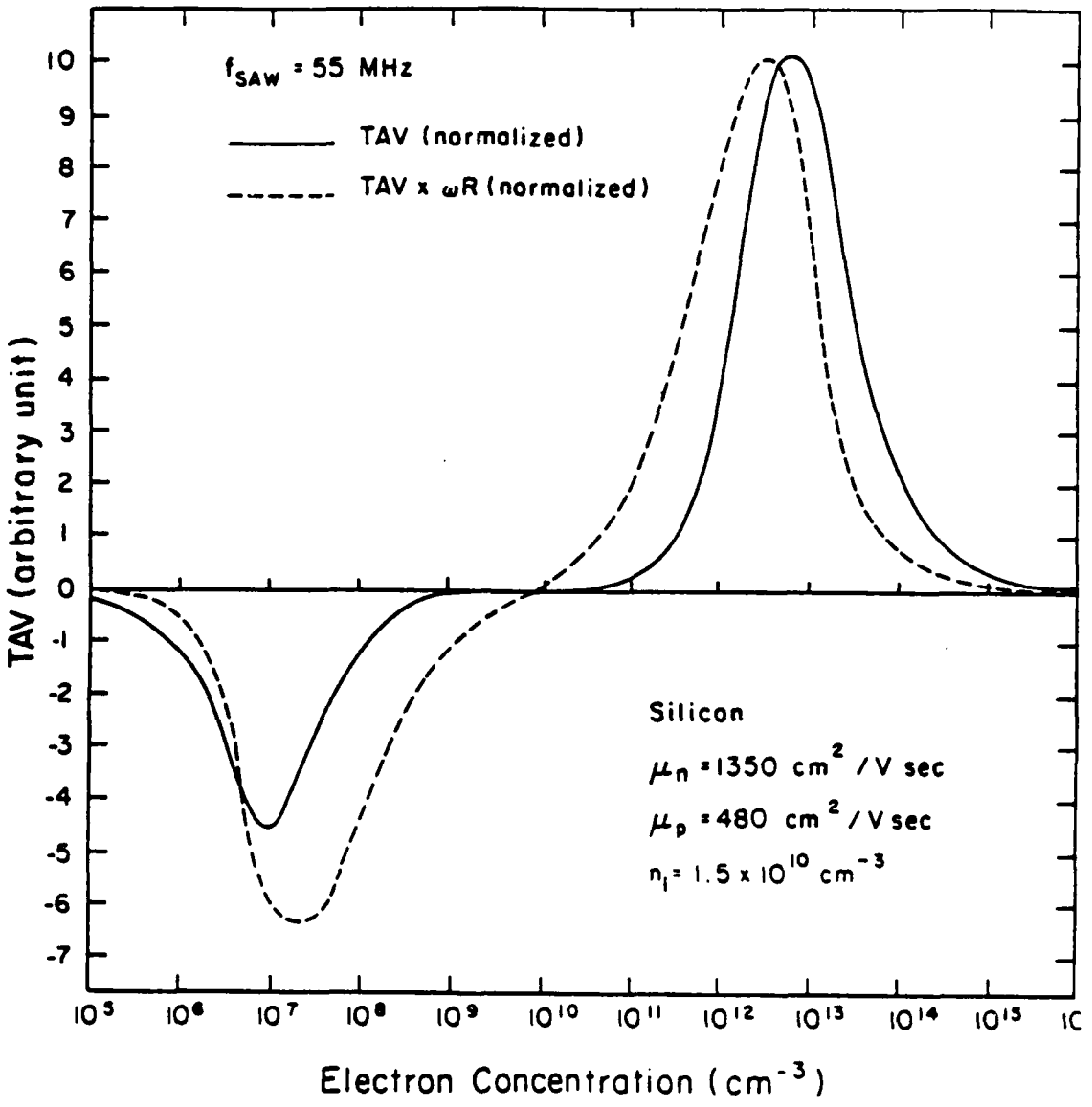

Figure 2.3b Transverse acoustoelectric voltage amplitude as a function of carrier concentration in silicon, SAW frequency = 55 MHz.

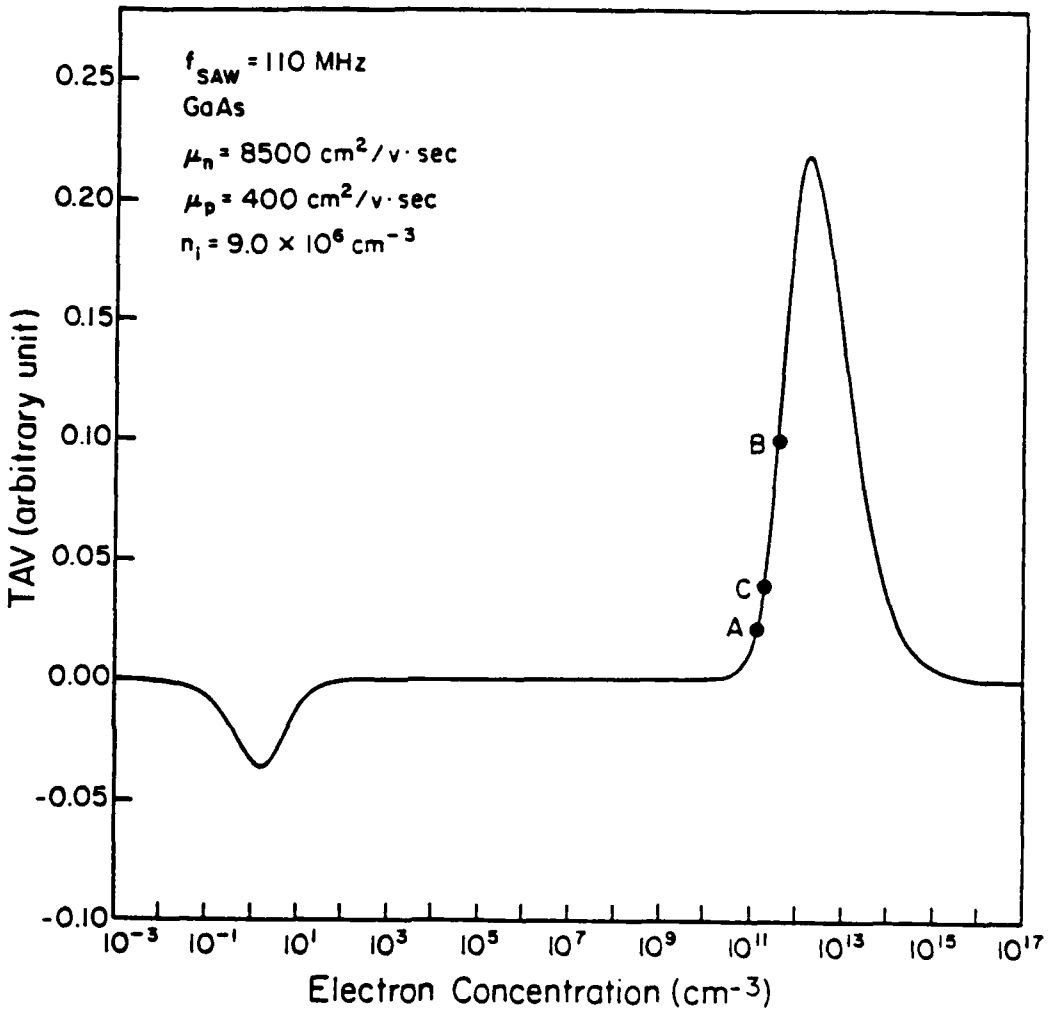

Figure 2.4 Transverse acoustoelectric voltage amplitude as a function of carrier concentration in GaAs.

surface conductivity exhibits a positive TAV and vice versa for p type. 2) There is a maximum in both n and p regions because at near intrinsic concentrations there are few carriers to interact with the electric field and at very high concentrations the free carriers effectively screen the probing electric field and the TAV amplitude reduces. Thus by monitoring the TAV amplitude one can distinguish between electron and holes surface conductivities and also obtain the magnitude of the free carrier concentration.

One should note the high sensitivity of the TAV signal at very low carrier concentrations which extends the measurement capability to very high resistivity materials such as Cr doped GaAs ($\rho > 10^7\,\Omega\,cm$). This is an advantage over other measurement techniques such as C-V or four point probe measurements. On the other hand the sensitivity of the TAV technique decreases at very high carrier concentrations and surface characterization with average surface resistivity below $0.01\,\Omega\,cm$ is not practical. Lock in detection of the TAV amplitude has alleviated this problem to some extent. It should be noted that in this work the surface characterization is referred to the region with a thickness on the order of the semiconductor extrinsic Debye length or the acoustic wavelength whichever is shorter.

CHAPTER 3

TAV MEASUREMENTS UNDER APPLIED BIAS VOLTAGE

In this chapter a discussion of the new delay line structure which allows the modulation of the surface potential via a small external bias voltage (± 10 volts range) is presented. Development of the theoretical foundations which are utilized in the TAV versus voltage (TAV-V) measurements are discussed next. The subjects to be presented are as follows:

- New delay line structure for TAV-V measurements.
- A depth profiling procedure which is applicable to the measurements where the free carrier concentration is the primary measured quantity rather than the depletion layer width.
- Evaluation of the interface charge density and flat band voltage by comparing theoretical and experimental TAV-V curves.
- TAV transient measurements and the estimation of the carrier lifetime and surface generation velocity.

3.1 A New Delay Line Structure for TAV-V Measurements and the Experimental Apparatus

The delay line arrangement is shown in figure 3.1. The piezoelectric substrate is a y cut z propagating $LiNbO_3$ with two aluminum interdigital transducers fabricated on the surface (fig. 3.1a). The semiconductor is placed above the $LiNbO_3$, with the surface under study facing the $LiNbO_3$. In the previous work the

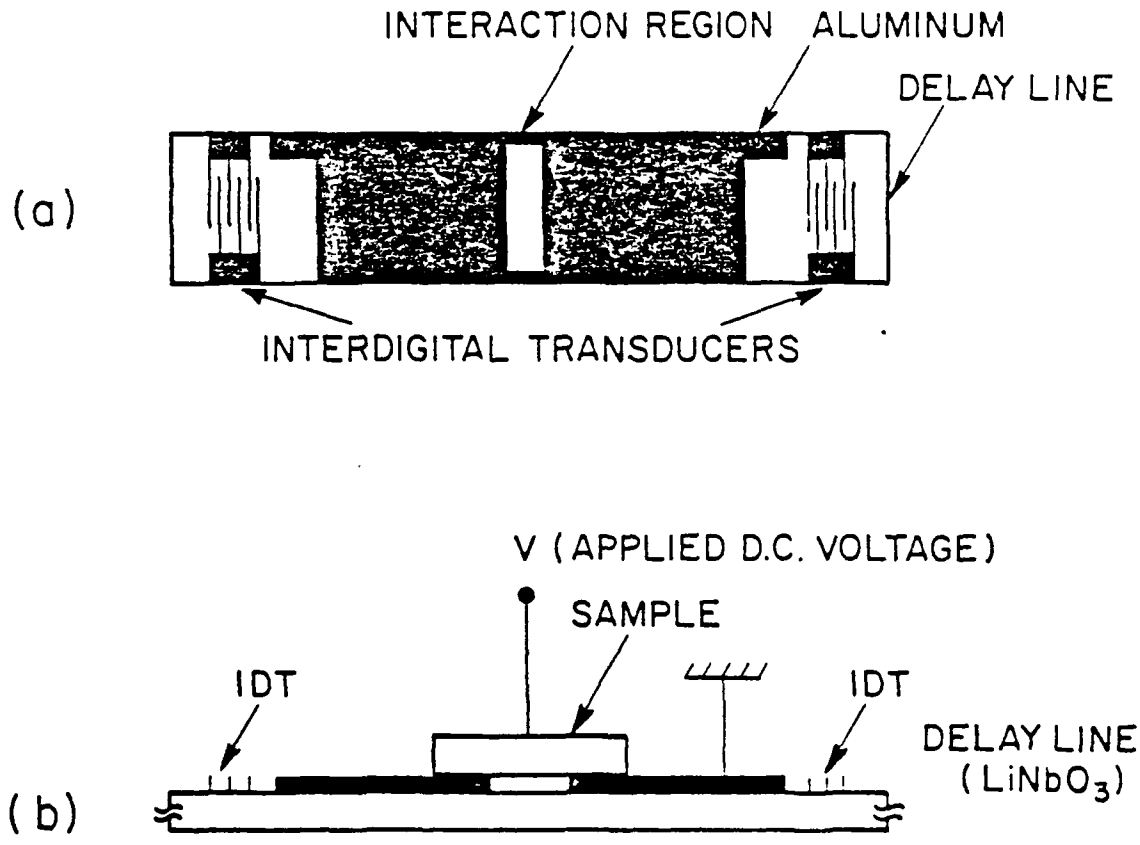

Figure 3.1 Delay line arrangement for TAV measurements.

TAV signal across the semiconductor has been detected by placing an aluminum plate on the back surface of the semiconductor and another one under the $LiNbO_3$ [42] (fig. 1.1a). The TAV is a dc voltage across the semiconductor, therefore in order to monitor this signal through the insulators such as the oxides on the semiconductor surfaces and the $LiNbO_3$, the rf voltage and thus the probing electric field are pulsed. As a result the TAV can be detected as a transient voltage via the capacitive coupling [50,71]. In the new TAV measurements a thin aluminum structure ($\simeq$ 1 μm) is evaporated on the $LiNbO_3$ surface as shown in figure 3.1a [50]. This structure provides a ground path for the TAV signal which does not pass through the $LiNbO_3$ substrate, as compared to the previous work. At the center of the aluminum structure a window is made to provide an interaction region (fig. 3.1a). The mechanical surface wave produced by the interdigital transducer is accompanied by the probing electric field only in the region not covered by the aluminum. Under the aluminum covered area the electric field tends to zero while the mechanical wave continues to propagate. Once the mechanical wave reaches the interaction window the probing electric field is regenerated. The area of the semiconductor surface which is to be tested is placed above the interaction region (fig. 3.1b) where the probing electric field penetrates in the semiconductor surface, interacts nonlinearly with the free carriers and produces the TAV signal.

In order to change the surface potential, the bias voltage is applied across a contact to the semiconductor back surface and the ground path underneath the surface under study. The nature of these contacts are important for a nondestructive measurement. The back contact can be provided by removing the possible insulator layer from the back surface and evaporating an appropriate metal with no hot step involved (e.g., by contacting to an abraided region on the back surface) to form an ohmic contact. The formation of the back ohmic contact is not necessary for the TAV detection, since the probing rf electric field only interacts with the carriers at the surface under study (as long as the extrinsic Debye length is smaller than the semiconductor thickness). If the insulator layer is not removed from the back surface, then the voltage drop across this layer and the variation of the back side surface potential should also be considered in evaluating the device side surface potential as a function of the bias voltage. The contact to the surface under study (device side) is of special importance. This contact is simply provided by placing the semiconductor (with or without an insulator layer) on the Aℓ coated $LiNbO_3$ as shown in fig. 1(b) and there is no processing involved. If there are no insulators present in the signal path, a dc current can pass through the detection system. In this case the measurement apparatus can be adapted to monitor the steady state current density ($J_d(y)$ in 2.23) instead of the TAV. The important features of the new delay line structure are shown in fig. 3.2a which

includes: 1) The interaction region width (w_i) which determines the spatial resolution of the measurement. For higher spatial resolution a smaller width (w_i) is desired, but a lower limit is set by the detection sensitivity of the TAV signal. w_i also affects the form of the bias electric field (should be distinguished from the rf probing electric field) which passes through the area under study. As shown in figure 3.2a the probed area is the only region where the aluminum ground is removed from the $LiNbO_3$ substrate. Thus the bias electric field bends towards the corners of the interaction window and the center of the probed region is unaffected. The surface potential in this region (thickness = w_u in figure 3.2a) can only be slightly modulated as compared to the edges of the probed area. Therefore the calculated surface potential for a certain bias voltage can be considerably different from the real value. To lessen this problem, w_u should be reduced as much as possible by such means as the reduction of w_i to its experimental limit (detection sensitivity). The aluminum ground path thickness (t_a) can also be increased in order to obtain a more uniform electric field. For practical vacuum deposition, t_a does not exceed a few microns. Also the amplitude of the mechanical surface waves might be reduced by the thick aluminum loading effect to such an extent that the regenerated probing electric field is not adequate to produce a detectable TAV signal. One remedy is to use an array of aluminum fingers (figure 3.2b), all connected to a common ground terminal with spacings (w_{ie}) on the order of

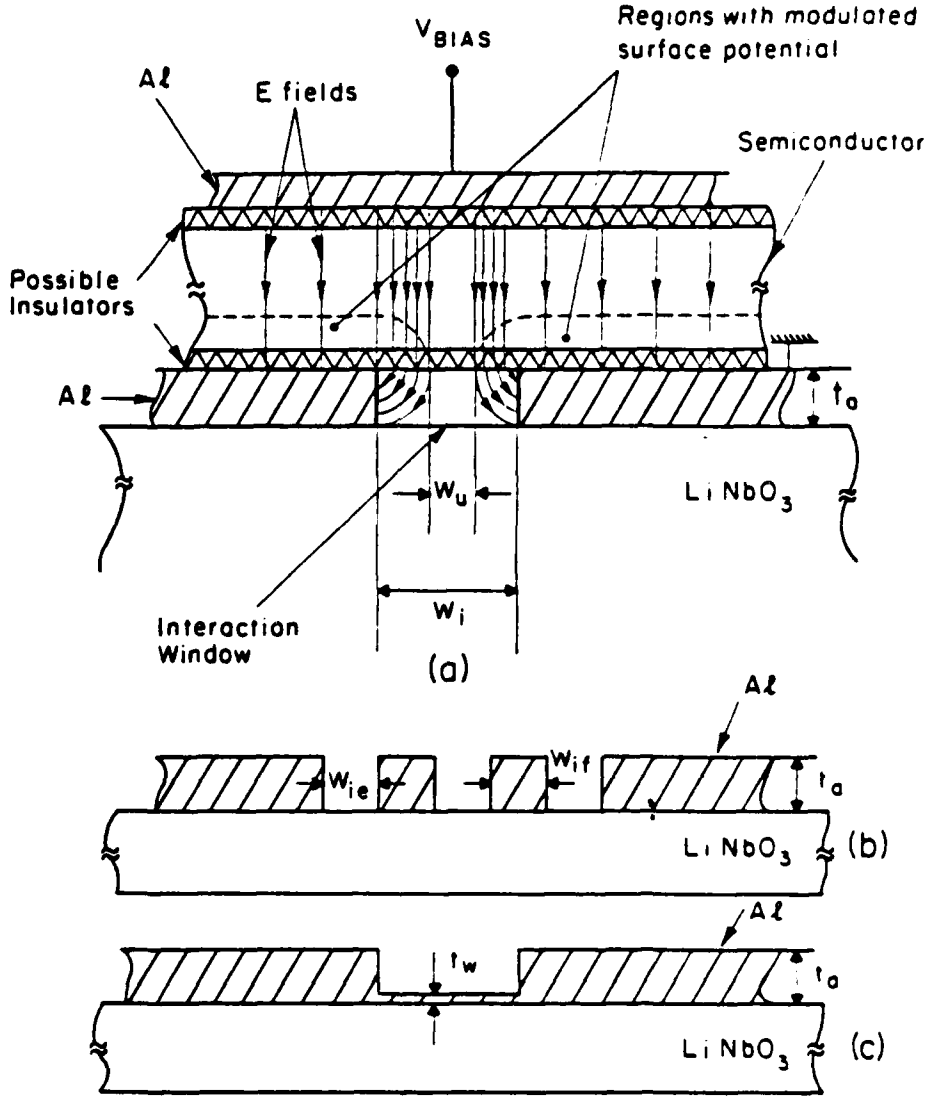

Figure 3.2 Different arrangements of the new delay line structure.

$2t_a$ or smaller. In this case an almost uniform surface potential modulation is possible without the reduction of the TAV signal. The spatial resolution cannot be improved by this structure since the total interaction region area (the sum of the spacing between fingers) is still determined by the TAV detection sensitivity and the spatial resolution is further reduced by the addition of the nonzero width of the aluminum fingers (w_{if}). In the experimental work reported in this thesis the one piece interaction window with a width on the order of mm is used. Another method to establish a more uniform bias field is to leave a very thin aluminum layer with a thickness (t_w) on the order of 100 A^o in the interaction region (figure 3.2c). This layer should be thin enough to allow the probing rf field to pass through it without excessive attenuation. The bias electric field can then be terminated on the thin Aℓ layer, producing a uniform electric field. In this work the thickness of the aluminum ground path is about 1 μm. The interaction region width also determines the lower limit of the TAV transient measurements as will be discussed in the following sections. This limit is established by the transit time of the surface acoustic wave through the interaction window (≃ 0.3 μsec per mm). If placing the wafer on the piezoelectric substrate is not desirable, an air gap can be maintained between the surface under study and the substrate by the proper mechanical arrangement, resulting in a contactless measurement. The air gap should be considerably smaller than the acoustic wavelength which is on the

order of 32 or 64 μm for 110 or 55 MHz SAW frequencies respectively. The optical lithography tools, used for proximity exposure [115] which are capable of maintaining a small gap in the range of 10 to 25 μm can be used for this purpose. In this case the voltage drop across the air gap should be accounted for in calculating the surface band bending by the bias and rf fields. This arrangement can also aid the uniformity of the bias electric field.

The experimental apparatus for the TAV-V measurements is shown in figure 3.3. The setup is divided into four sections as follows: section I consists of the electronics which generate the rf pulse, section II is arranged to apply the bias voltage across the semiconductor and measures its value, TAV detection is performed by section III and section IV is the SAW delay line structure which has already been discussed. The rf pulse is generated by modulating the output of a continuous rf source by a pulse generator. Modulation is performed by a balanced mixer. Typical rf frequencies are 55 MHz or 110 MHz. Pulse width ranges from a fraction of μsec to 10 msec and the pulse period can vary between 0.5 msec to 500 msec. The rf pulse is fed to an rf amplifier followed by an attenuator which keeps the rf pulse amplitude in the range of 10 volts peak to peak. The amplified rf pulse is then applied to the interdigital transducer (IDT) which is tuned to be a 50Ω resistive load at the desired frequency. The IDT by itself is a capacitive load and a single series inductance is used for tuning. The application of the rf pulse to the input IDT launches the surface acoustic wave.

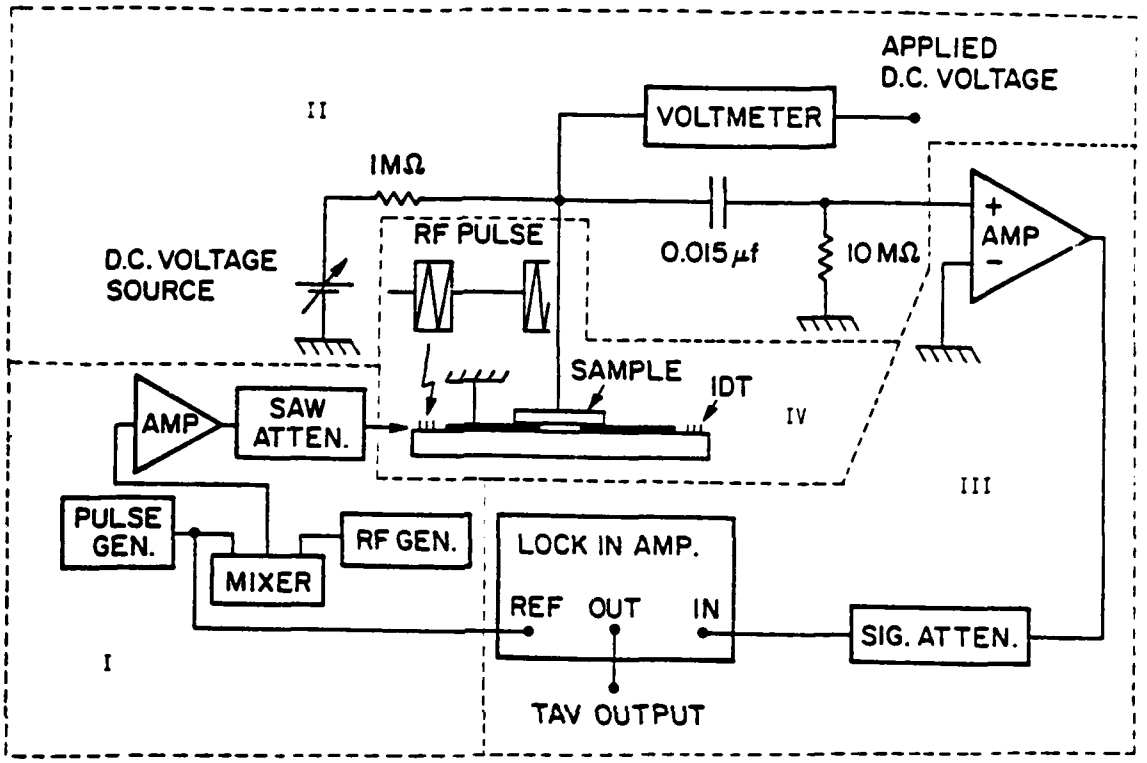

Figure 3.3 TAV versus voltage measurement experimental apparatus

Section II shows the arrangement which allows the biasing of the sample and the simultaneous detection of the TAV signal. It consists of a dc voltage source (can also be a pulsed voltage source) in series with a high value resistance which effectively constitutes a current source, connected to the semiconductor back surface. The high value resistor is used to prevent the shorting of the TAV signal by the low output impedance voltage source. The TAV signal is applied to a low frequency amplifier via a capacitor. The aluminum structure under the semiconductor is grounded and the applied bias voltage is measured at the semiconductor back surface (similar to substrate bias in MOS) by a voltmeter with an analog output. It is also possible to apply the bias voltage directly to the aluminum structure instead of grounding it (similar to gate bias in MOS). In this case the back surface can be at a virtual dc ground through the input of the amplifier if the 0.015 μf capacitor is removed. This configuration is not used because of the uncertainty in the ground voltage. Also the saturation of the amplifier by the possible dc input causes additional problems. The advantage of this configuration (if it is used after careful examination) is that it requires a smaller bias voltage range than the previous arrangement. To detect the TAV amplitude (section III in figure 3.3) the TAV signal is fed to a low frequency amplifier with the maximum bandwidth from dc to 10 MHz. The output of this amplifier is connected to the input of a lock in amplifier, possibly via a signal attenuator. The attenuator is sometimes used

to eliminate the readjustment of the amplifiers at different signal levels. The reference signal to the lock in amplifier is provided by the pulse generator. The TAV waveform for a p type, 11-16 Ω cm silicon sample is shown in figure 3.4. To obtain the TAV-V curves, the amplitude of the TAV signal is recorded as a function of the applied bias voltage, as the voltage source is scanned in the desired range. In the TAV transient time constant (τ) measurements, the lock in amplifier can be replaced by a computer which calculates the time constant, and (τ-v) is recorded. The bias voltage source can be either dc (a slow varying ramp) or pulsed. In most of the following experiments a slow varying ramp is used and the operation under pulsed bias voltage is also discussed.

3.2 New Depth Profiling Procedure

Electrical depth profiling is most commonly performed by differential capacitance-voltage (C-V) techniques [53-56] and other capacitance measurements such as feedback method [57] and second harmonic technique [116]. The common characteristic of all these measurements is that the depletion width (W) is monitored as a function of the bias voltage (V) by measuring the depletion layer capacitance. The average majority carrier concentration profile, (for example $\hat{n}(x)$ in n type semiconductor), and from that the dopant density profile (N(x)), are then evaluated by the mathematical manipulation of the depletion width versus voltage (W(V)) [53-56] or by producing a capacitance related signal which is proportional to N(x) or 1/N(x) [57-116]. In this section the profiling

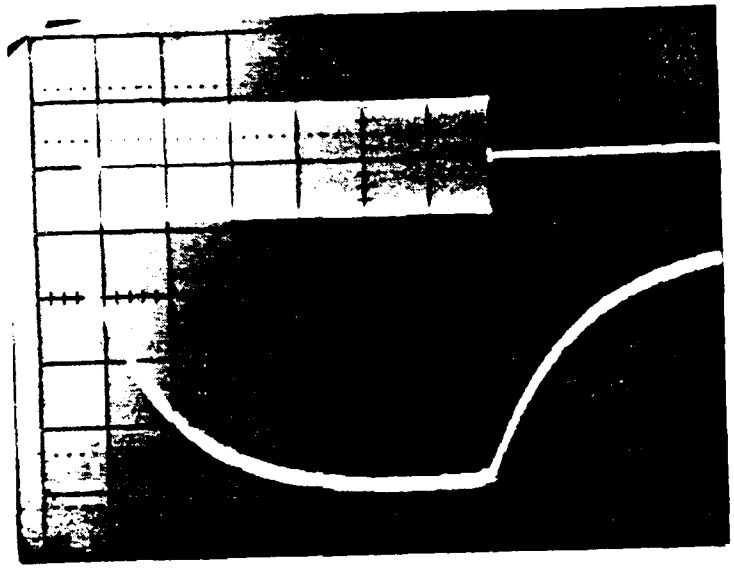

Figure 3.4 Experimental TAV Waveform
(Si sample, p type, ρ = 11-16 Ω cm)
Upper trace: Rf pulse, vertical scale = 5V/div,
Horizontal scale = 100 μsec/div.
Lower trace: TAV signal, vertical scale = 1 mv/div.,
Horizontal scale = 100 μsec/div.

capability of the measurements which are primarily sensitive to the free carrier concentration rather than the depletion layer thickness is introduced [51,52]. Using this procedure, the techniques measuring such parameters as surface conductance and surface photovoltage [106], optical reflection [117], transverse acousto-electric voltage (TAV) [71] and Hall effect [118], which are presently used to characterize semiconductor materials might be suitably adopted for depth profiling. Semiconductor properties, e.g., mobility, trap and ionized impurity energy levels and density which are measurable by the above methods might also be evaluated as a function of depth in addition to the dopant density profile. The experimental setup for these measurements should be capable of monitoring the carrier density at the edge of the depletion layer, considering the abrupt space charge edge (ASCE) approximation.

The surface potential is varied by the bias voltage, and the average carrier concentration versus the applied bias voltage is monitored ($\hat{n}(V)$). The information about the depletion layer width versus the bias voltage ($W(V)$) can then be obtained from the mathematical analysis of the $\hat{n}(V)$ curve. This analysis is presented in section 3.2.1 which leads to the average free carrier concentration depth profile $\hat{n}(x)$. It should be noted that in the C-V technique also, the majority carrier concentration depth profile which is subjected to the Debye averaging effect [56] is measured rather than the impurity ions density profile [54,55]. The approximate doping profile can then be calculated by using the

computations discussed in references [55] and [56]. The same limitations and approximations are applicable in this work. The limitations, corrections and experimental implications are presented in section 3.2.2.

3.2.1 Theoretical Analysis

For depth profiling using the measurements sensitive to the free carrier concentration, one should obtain the depletion width as a function of the bias voltage (W(V)) [52]. In this analysis, the ASCE approximation is used, and it is assumed that the surface potential is modulated by a bias field, applied across an insulator on the surface and the substrate. The effects of the surface states and the minority carriers are neglected. An n type semiconductor is considered without losing the generality of the treatment. Poisson's equation is considered along the depleted region (figure 3.5).

$$\frac{d^2V(x)}{dx^2} = -\frac{q}{\varepsilon_s}\eta(x) \tag{3.1}$$

$$\eta(x) = N(x) - n(x) \tag{3.2}$$

where

$V(x)$ = electric potential

x = distance from the surface into the semiconductor

q = electronic charge

ε_s = semiconductor permitivity

$n(x)$ = majority carrier concentration profile

$N(x)$ = ionized dopant concentration profile

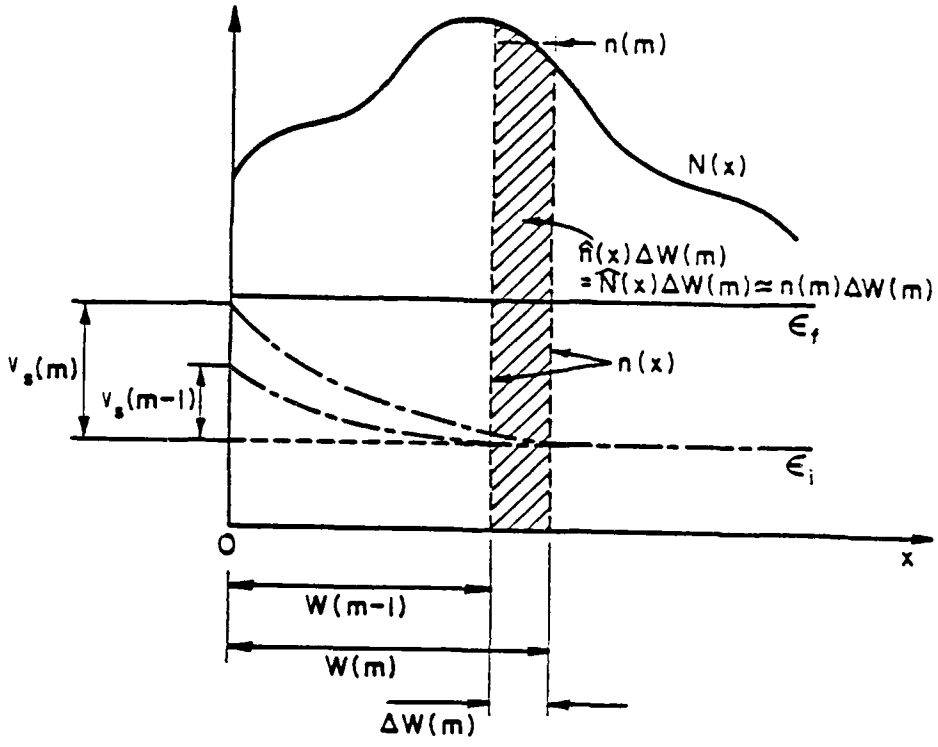

Figure 3.5 Surface potential and depletion width modulation by the applied bias voltage.

The ASCE approximation suggests

$$\left.\begin{aligned} n(x) &= 0 \qquad \text{for} \quad x \leq W \\ n(x) &= N(x) \qquad \text{for} \quad x > W \end{aligned}\right\} \tag{3.3}$$

where W is the depletion layer thickness. The boundary conditions at the depletion edge (W) and the surface are

$$\text{B.C.} \begin{cases} V(W) = 0 \\ V(0) = V_s, \quad V_s = \text{surface potential} \\ E(W) = \left.\dfrac{dV(x)}{dx}\right|_{x=w} = 0, \quad E = \text{electric field} \end{cases} \tag{3.4}$$

The applied bias voltage (V_B) can be written in the following form:

$$V_B = V_{FB} + V_i + V_s \tag{3.5}$$

where V_{FB} is the flat band voltage, and V_i is the voltage drop across the insulator due to the space charge. Therefore

$$V_i = \frac{Q_{sc}}{C_i} \quad , \quad Q_{sc} = \varepsilon_s E_s \tag{3.6}$$

where Q_{sc} is the space charge density per unit area, E_s is the electric field at the surface, and C_i is the insulator capacitance per unit area. Considering the boundary conditions in (3.4)

$$E_s = -\frac{q}{\varepsilon_s} \int_0^w n(x)\, dx \tag{3.7}$$

$$V_s = \frac{q}{\varepsilon_s} \int_0^w \int_w^t n(x)\, dx\, dt \tag{3.8}$$

using (3.5)~(3.8), it follows

$$V_B - V_{FB} = - \frac{q}{C_i} \int_0^w \eta(x)\, dx + \frac{q}{\varepsilon_s} \int_0^w \int_w^t \eta(x)\, dx\, dt \qquad (3.9)$$

Equation (3.9) is precise with no ASCE approximation and it can be applied to any doping profile. Knowing the value of $\eta(x)$ at any V_B, the value of W must be calculated. To do so the ASCE approximation and finite difference technique are used. A voltage increment (ΔV_B) is considered which results in a depletion width increment (ΔW). Using equation (3.9) for the mth voltage increment we find:

$$\Delta V_B(m) = V_B(m) - V_B(m-1)$$

$$= - \frac{q}{C_i} \int_{w(m-1)}^{w(m)} \eta(x)\, dx + \frac{q}{\varepsilon_s} \left[- \int_0^{w(m-1)} \int_{w(m-1)}^{t} \eta(x)\, dx\, dt \right.$$

$$\left. + \int_0^{w(m)} \int_{w(m)}^{t} \eta(x)\, dx\, dt \right] \qquad (3.10)$$

To approximate $\eta(x)$ at each voltage interval, the ASCE approximation (equation 3.3) is used and it is also assumed that the average carrier concentration ($\hat{n}(x)$) is equal to a constant ($n(m)$) in that interval. Thus

$$\hat{n}(x)\Big|_m = \hat{N}(x)\Big|_m = n(m) \qquad (3.11)$$

By substituting (3.11) in (3.10) the following equation can be obtained after the mathematical manipulation:

$$\frac{q\, n(m)}{2\varepsilon_s} (\Delta W(m))^2 + \frac{q\, n(m)}{C_i\, \varepsilon_s} [\varepsilon_s + C_i\, W(m-1)]$$

$$\times \Delta W(m) - \Delta V_B(m) = 0 \qquad (3.12)$$

where $\Delta W(m)$ is the mth depletion width increment and

$$W(m-1) = \sum_{n=1}^{m-1} \Delta W(n) \qquad \text{for } m \geq 2$$

In deriving equation (3.12) it is assumed that at the bias voltage equal to the flat band voltage the depletion layer width is zero. Another method to derive (3.12) from (3.9) which provides a better physical insight is to shift the origin (x=0) inside the semiconductor with the translation equal to the previous depletion width (figure 3.5). In this case the insulator capacitance (C_i) is replaced by another capacitance (C_T) which includes the depletion width capacitance (C_d). Therefore:

$$C_T = \frac{C_i C_d}{C_i + C_d} \tag{3.13}$$

or

$$C_T = \frac{C_i \varepsilon_s}{WC_i + \varepsilon_s} \tag{3.14}$$

Now for the mth interval, the following equation can be obtained directly from (3.9).

$$\frac{q\, n(m)}{2\, \varepsilon_s} (\Delta W(m))^2 + \frac{q\, n(m)}{C_T} \Delta W(m) - \Delta V_B(m) = 0 \tag{3.15}$$

Substitution of C_T from (3.14) in (3.15) leads to the equation (3.12). By measuring n(m) at each voltage interval, $\Delta W(m)$ and thus W(m) can be calculated from (3.12), leading to the depth profile $\hat{n}(x)$. The voltage increment ΔV_B can be chosen to be smaller for more accurate calculations within the experimental limits. These limits which dictate a spatial resolution on the order of a few

Debye lengths are discussed in the next section. In (3.12) the second order term can be neglected if

$$\frac{\Delta W(m)}{2} << \frac{\varepsilon_s}{C_i} + W(m-1) \quad , \qquad C_i = \frac{\varepsilon_i}{t_i}$$

where ε_i = insulator permitivity,

t_i = insulator thickness

Therefore

$$\frac{\Delta W(m)}{2} << \frac{\varepsilon_s}{\varepsilon_i} t_i + W(m-1) \tag{3.16}$$

Typically the inequality (3.16) is satisfied except for possibly the first few steps. Equation (3.12) can also be simplified if $C_i << C_d$ (thick insulator). In this case (3.12) reduces to (3.15) with C_T replaced by C_i and the recursive nature of (3.12) is eliminated [51]. The condition $C_i << C_d$ is satisfied when:

$$\frac{\varepsilon_s}{\varepsilon_i} >> W(m-1) \tag{3.17}$$

Inequality (3.17) is valid only in the first few intervals. In fact, (3.17) determines the upper bound of the depletion width, below which the simplified equation can be used.

3.2.2 Experimental Limits, Corrections and Implications

The average majority carrier concentration profile ($\hat{n}(x)$) can be obtained by the procedure explained in the previous section. The next step is to evaluate the ionized impurity distribution ($N(x)$) from $\hat{n}(x)$. A number of corrections and mathematical manipulations are devised for the C-V technique which are also applicable

in this work. The reason is that the C-V profiling also measures $\hat{n}(x)$ instead of N(x) as pointed out in [54-56]. These corrections and other limitations such as the effect of interface traps at small depletion widths (which dictates the use of a higher measurement frequency) are discussed and the possible arrangements to reduce these limitations are considered.

The ASCE approximation divides the semiconductor in two distinct regions, one is the depletion region with no majority carriers and the other is the neutral region where the majority carrier concentration is equal to the impurity atoms density. In reality if there is a spatial variation in the ionized impurity distribution (N(x)), then the majority carrier profile (n(x)) cannot follow N(x) and a significant deviation can be present at the high concentration gradient regions. The reason is that at equilibrium, the total current inside the semiconductor which is the sum of the drift and diffusion currents is assumed to be zero. Diffusion of the mobile carriers from high to low concentration region has to be canceled by a drift current which is caused by an electric field in the opposing direction. This electric field is established by the deviation from charge neutrality which means that n(x) and N(x) cannot be equal. Also it can be deduced that the variation of the impurity profile is always sharper than the free carrier concentration profile. As an example, figure 3.6 shows a high-low abrupt profile for N(x) which varies from N_h to N_ℓ in a small distance compared to the local Debye length $L_D = \left(\frac{\varepsilon_s K_B T}{q^2 n(x)}\right)^{\frac{1}{2}}$.

N(x) ionized deposit concentration

n(x) majority carrier concentration

$\Delta\hat{n}(x)$ carrier concentration increment produced by an increment of bias voltage

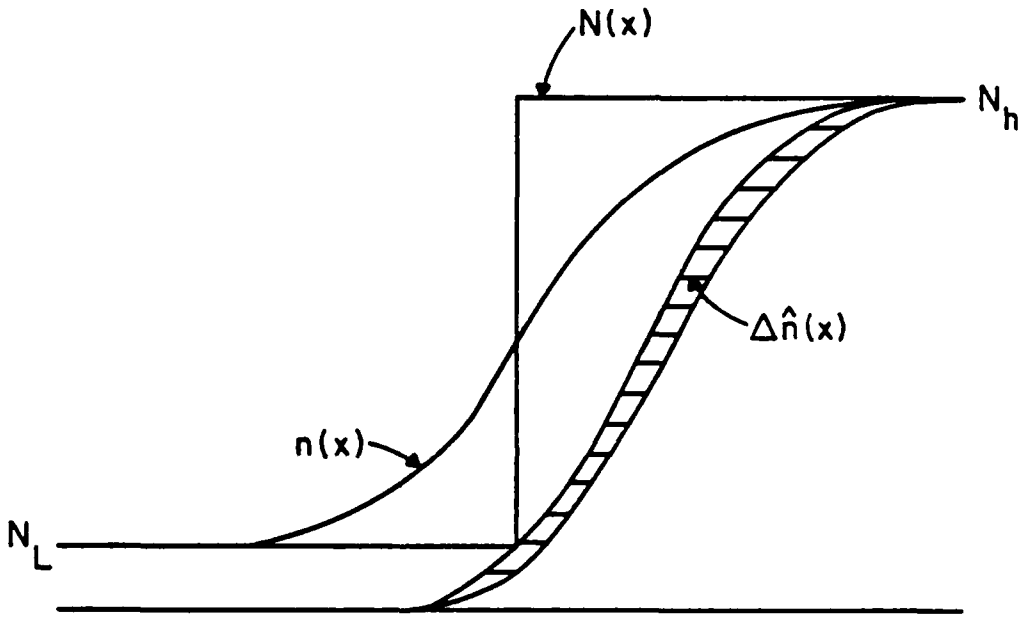

Figure 3.6 Ionized dopant density and majority carrier concentration profiles, near a high concentration gradient region.

The majority carrier profile is also shown (n(x)) which exhibits a lower gradient. The n(x) varies from high to low value in a distance on the order of a few extrinsic Debye lengths. If the measurement actually monitors n(x), then there is an equation from which N(x) can be obtained. This equation which is the result of equating drift and diffusion currents is as follows [55]:

$$N(x) = n(x) + \left(\frac{K_B T}{q}\right)\left(\frac{\varepsilon_s}{q}\right)\frac{d}{dx}\left[\frac{1}{n(x)}\frac{dn(x)}{dx}\right] \qquad (3.18)$$

Equation (3.18) can be applied to n(x) without a complicated computation scheme. But it is pointed out that the carrier concentration profile in itself is subject to the Debye averaging effect which leads to inaccurate results in the range of a few Debye lengths around the regions with sharp spatial variation of carrier density [56]. By incrementing the depleting bias voltage, $\Delta\hat{n}(x)$ is measured rather than the $\Delta n(x)$ as shown in figure 3.6. Extensive computer calculations are carried out to demonstrate this effect [56] and the results indicate that N(x) can be calculated from $\hat{n}(x)$(equation 3.18) reasonably well if N(x) varies gradually over a few Debye lengths. Other attempts are also made to relax the ASCE approximation [119-121] (using better approximations for $n(x)$ in (3.2)) but a general solution to the problem is too complicated to be practical. Thus in order to obtain N(x) from the measured profile, equation (3.18) can be used as a first correction step and then iterative computer solutions should be applied if a high spatial resolution is required in the high concentration gradient region

(deconvolution of the Debye averaging effect). The flow charts of the depth profiling procedures and corrections, applicable to this work and the C-V technique are shown in figure 3.7.

The treatment presented in section 3.2.1 neglects the effects of minority carriers and interface states. The validity of these assumptions should be examined. The interface states response can affect the measurement in two ways. First if the interface states trap charges (Q_{it} = coul/cm^2) respond to the perturbation which is used as the probing tool. For example, in C-V technique a 1 MHz sinusoidal signal is used to monitor the depletion layer capacitance. If the response time of the interface traps is lowered to the range of μsec, then they can contribute to the total measured capacitance and distort the data [58]. The interface states response time is reduced if the depletion layer width decreases (going towards flat band), due to the increase of the majority carrier concentration (figure 3.8). Thus at a fixed measurement frequency the density of interface trap levels (D_{it} = cm^{-2} eV^{-1}) and their capture probability can be the dominant factor in determining how close to the surface the depth profile can be obtained without an excessive error. This limit can be reduced by decreasing D_{it} or increasing the measurement frequency. The TAV measurement reported in this work is inherently a high frequency measurement, thus it has the advantage that the interface states preclude response at frequencies that the interaction between the probing electric field and the free carriers takes place (in the

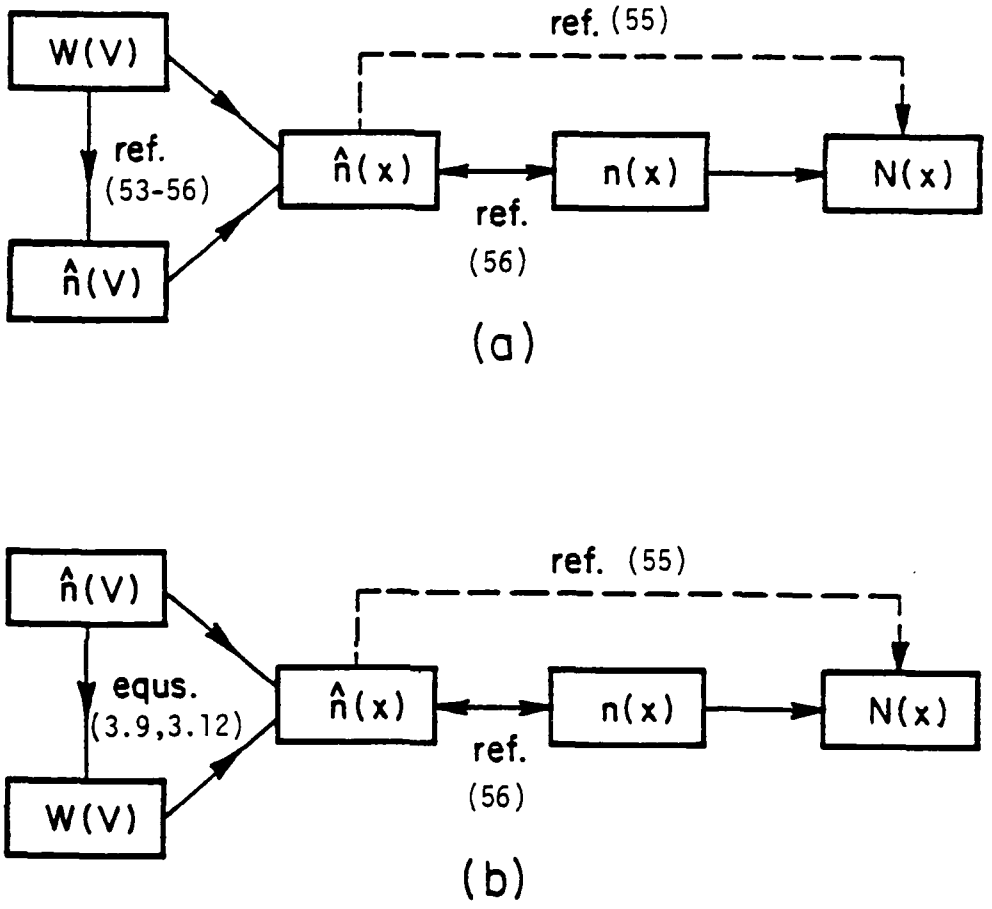

Figure 3.7 The profiling procedure for (a) C-V technique and (b) this work [52].

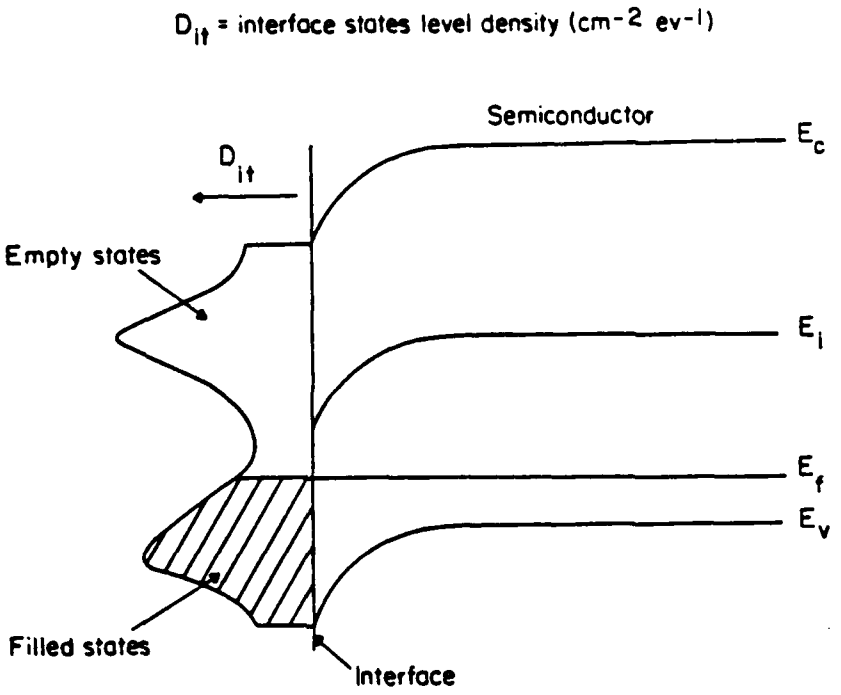

Figure 3.8 Filled and empty interface states at a certain surface potential.

range of 100 MHz). Therefore the profiles closer to the surface can be obtained (as compared to the C-V measurement) without added complexity (such as corrections for high frequency interface states response or complicated phase sensitive measurements at high frequency). It should be mentioned that the interface states can affect the transients of the TAV signal as will be discussed in the later sections.

Secondly, the interface states can affect the profiling by responding to the bias voltage which is used to modulate the depletion width. If a slow varying ramp voltage is used, then there is enough time for the charge occupancy of the interface states to change as they pass through the Fermi level (figure 3.8). Therefore these charges contribute to the total space charge and affect the surface potential modulation at any bias voltage. As a result there will be a stretch out along the bias voltage axis [58, 113] and the true depletion width cannot be calculated without considering the interface states charge occupancy variation. The equation relating the bias voltage to the surface potential (3.5) should then be modified to account for the interface states charges. One experimental method to solve this problem is to use a pulsed bias voltage. In this case if the pulse width is shorter than the interface traps response time, then they cannot change their charge occupancy fast enough and the correct depletion width can be obtained. To use the pulsed bias arrangement, the detection apparatus should be able to reach its steady state long before the end

of the bias pulse. Another advantage of the pulsed bias is to eliminate the effect of minority carriers. If a dc bias field is used, the maximum depletion width (W_m) is determined by the onset of inversion which is set when the surface potential exceeds twice the difference between the Fermi level and midgap in the semiconductor bulk. As an example, W_m is about 1 μm for a 10^{15} cm^3 doped silicon. To obtain the depth profile beyond W_m, the pulsed bias can be used. In this case the measurement is performed in a time scale shorter than the time required for the minority carriers to build up in the inversion layer (τ_r). Since τ_r is usually longer than the interface traps time constant (τ_r can be on the order of tens of seconds for good quality silicon), the width of the bias pulse is determined by the interface traps response time (in silicon). Therefore by using the pulsed bias, the formation of inversion layer is eliminated and the profiling depth can be extended to a new limit, determined by the avalanche breakdown. As an example, the maximum depletion width before the avalanche breakdown is about 10 μm for a 10^{15} cm^{-3} doped silicon and it decreases as the dopant concentration goes up. In TAV measurements the pulsed bias can be used by replacing the dc voltage source in Figure 3.3 with a pulse source. The bias pulse can be triggered at about the same time as the rf pulse and its pulse width is determined by the time constant of the interface traps (i.e., τ_{nit} or τ_{pit} where $\tau_{nit} = (C_{nit}\, n_s)^{-1}$, C_{nit} is the electron capture probability and n_s is the electron concentration at the surface [58]).

It should be noted that in depletion condition which is used for profiling, the interface trap effect is stronger than the bulk trap as long as the weak inversion condition is not established. This effect will be discussed in more detail in the following sections. In C-V measurements one method to account for the interface trap stretch out effect, is the high, low frequency C-V measurement [122].

Another parameter to be considered is the flat band voltage (V_{FB}) used in equation (3.9). This voltage is in fact a reference point which marks the zero depletion width condition. Obtaining the exact V_{FB} at any general doping profile might not be feasible, but for most of the experimental cases in practice, a good approximation of V_{FB} can be obtained. For example, for implanted Si samples with thermal oxide, the oxide charge is almost invariably positive. Therefore if the implant is n type, the surface tends to be close to accumulation or flat band at zero bias (this case is experimentally demonstrated in the next chapter). If the implant is p type then the surface tends to be depleted, and V_{FB} can be approximated by estimating the dopant concentration at the surface. The oxide charge can be estimated from the data, obtained for the samples with similar oxidation process but with uniform doping. Therefore a reasonable estimate for V_{FB} can be found by trial and error.

In the profiling procedure presented in this section, since the information about the depletion layer thickness is obtained from

the n(V) data, the fabrication of MOS or p-n or Schottky-barrier structures on the semiconductor is not always necessary. However, appropriate provisions should be made to vary the surface potential. Methods such as the polarization of the semiconductor electrode in contact with a suitable electrolyte [100,104] might be used. The surface potential can be modulated by applying the bias voltage between the semiconductor and a counter electrode immersed in the same electrolyte, or by passing a small current through the semiconductor and counter electrode, while measuring the voltage drop between the semiconductor and a third reference electrode. In some cases, surface potential can be varied by changing the chemical composition of the species at the semiconductor surface. In the nondestructive test, monitoring the TAV, the bias voltage is applied to the semiconductors by placing them between two aluminum field plates, as discussed in section 3.1. The carrier concentration depth profiling of the phosphorous implanted high resistivity p type silicon substrates by TAV measurements, is presented in the next chapter.

Signals related to phenomena such as surface photovoltage, reflectance, and Hall effect are sensitive to the free carrier concentration. These techniques can be adapted for impurity depth profiling if the appropriate setup is constructed to vary the surface potential while the carrier concentration at the depletion edge is monitored. In addition, parameters such as carrier mobility, trap energy levels, density and capture cross section can be

profiled using these measurements. In these cases, the desired parameter should be measurable in addition to the carrier concentration, for example by spectroscopic or transient techniques. As an example, the interface states energy levels have been studied by TAV spectroscopy [47,85, Chapter 5 of this thesis]. Using the same method, combined with the profiling procedure, a depth profile of the interface states band structure can be obtained.

3.3 Evaluation of the Interface Charge Density and Flat Band Voltage for Uniformly Doped Semiconductors Using Theoretical and Experimental TAV-V Curves

The purpose of this section is to present both the theoretical and experimental aspects of the TAV amplitude versus voltage (TAV-V) measurements which leads to the nondestructive evaluation of the interface state charges and flat band voltage [50]. Unlike the previous section, the theoretical discussion is combined with the experimental data in this section (for uniformly doped and thermally oxidized silicon samples). The reason is that the nature of the approximations and the general approach can be pointed out more clearly by comparing the theoretical and experimental results in the same section. The flat band voltage (V_{FB}) is the voltage applied across the semiconductor which produces no band bending (zero surface potential) from the semiconductor bulk, up to its surface (using any form of structure, e.g., MIS, p-n junction, Schottky barrier, semiconductor/electrolyte, etc.). The V_{FB} is an important parameter for semiconductor devices because it is an

indication of the surface potential at zero bias condition. As an example, in MOS transistors, V_{FB} offsets the threshold voltage which is the key parameter in device design. In the following discussions the effect of silicon/oxide interface on the flat band voltage and its determination are discussed. The main contributors to V_{FB} in this case are the oxide fixed charges (Q_f) and the difference between the gate metal and Si work functions (ϕ_{ms}).

To estimate the interface charge density the comparison between the theoretical and experimental TAV-V curves is used. To obtain the theoretical TAV-V plot, the average free carrier concentration in the space charge is calculated at each surface potential (shown as V_s in the inset of figure 3.11). Then the space charge region of the semiconductor is created as a region with the calculated average free carrier concentration, but at flat band condition. The reason for this approach is that the theoretical dependence of the TAV amplitude on the free carrier concentration (equation (2.40)) is obtained, assuming a near flat band condition. The normalized TAV amplitude as a function of surface potential (TAV-V_s) can then be calculated. Knowing the oxide thickness, the dependence of the surface potential on the applied bias voltage (V_B) is obtained (at zero or a fixed value of Q_f and ϕ_{ms}). Then the theoretical TAV versus bias voltage (TAV-V_B) is calculated. The detailed discussion of the above procedure and the methods to extract the interface charge density are discussed in the following sections.

3.3.1 Determination of the Theoretical TAV-V_s

The block diagram of the TAV versus V_s calculation is shown in figure 3.9 (section I). The steps taken, are as follows:

1) determination of the excess hole and electron concentration in the space charge region as a function of the surface potential [106,107]. The form of the band bending and the symbols used in the following calculations are shown in the inset of figure 3.11. The excess electron and hole concentrations are:

$$\Delta n_{2d} = \int_0^\infty (n - n_b)\, dx \tag{3.19}$$

$$\Delta p_{2d} = \int_0^\infty (p - p_b)\, dx \tag{3.20}$$

where Δn_{2d} = excess electron concentration per unit area

Δp_{2d} = excess hole concentration per unit area

n_b, p_b = equilibrium electron and hole concentrations per unit valume in the semiconductor bulk (quasi neutral region)

n, p = equilibrium electron and hole concentrations per unit volume in the space charge region

x = distance from the surface into the semiconductor.

The distinction between space charge and neutral region is obviously that in the former the charge neutrality is not satisfied and in the latter it is, but in both regions it is assumed that $np = n_i^2$.

By changing the variable in (3.19) and (3.20) from x to u we have

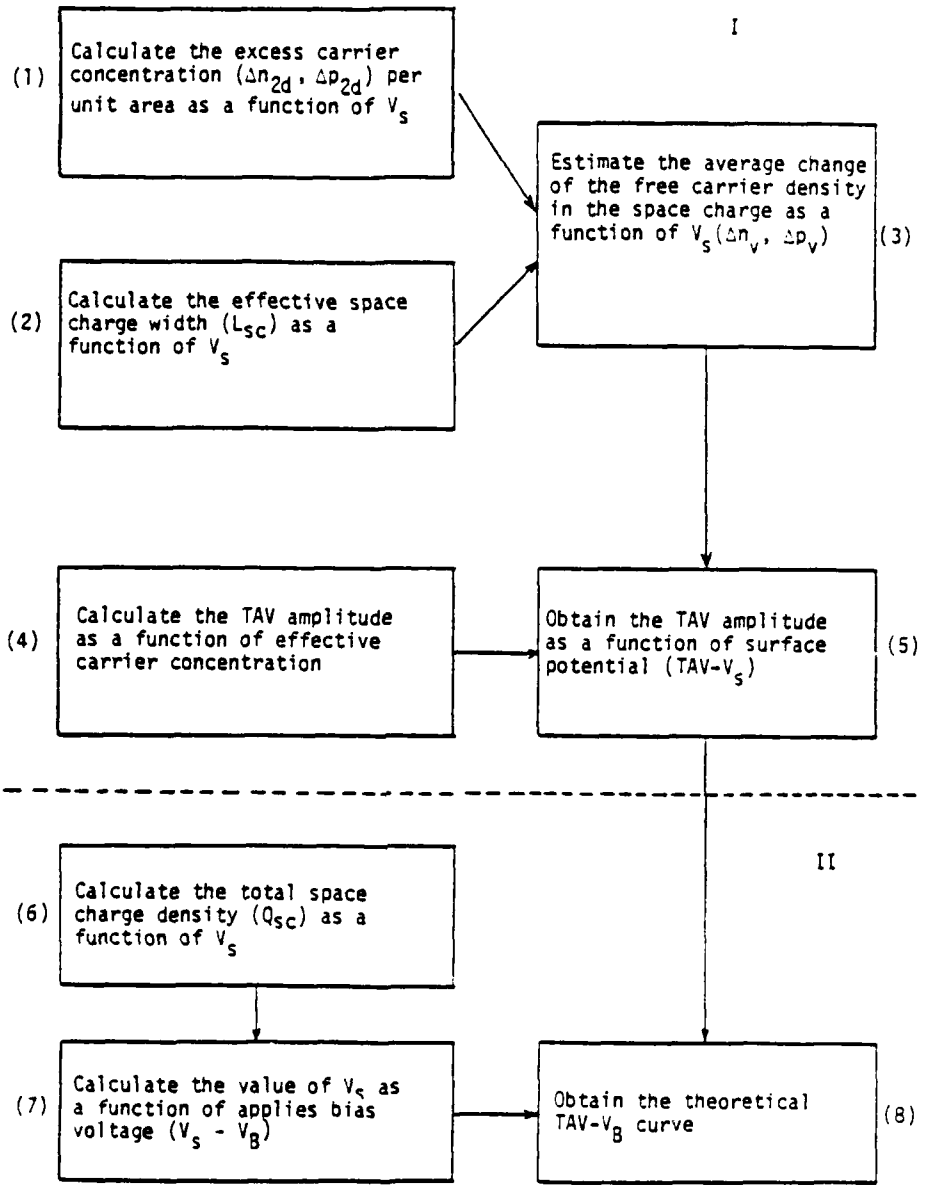

Figure 3.9 Block diagram of the TAV amplitude versus voltage, calculation procedure.

$$\Delta n_{2d} = n_i L_i \int_{u_s}^{u_b} \frac{e^u - e^{u_b}}{F(u, u_b)} du \tag{3.21}$$

$$\Delta p_{2d} = n_i L_i \int_{u_s}^{u_b} \frac{e^{-u} - e^{-u_b}}{F(u, u_b)} du \tag{3.22}$$

where $u = \frac{q}{K_B T} \phi$, $u_b = \frac{q}{K_B T} \phi_b$, $u_s = \frac{q}{K_B T} \phi_s$ (figure 3.11)

and ϕ_b = potential difference between the Fermi level and the intrinsic Fermi level in the bulk

ϕ = the same as ϕ_b but at point x

ϕ_s = the same as ϕ_b but at the surface

n_i = intrinsic carrier concentration

$L_i = \left(\frac{\varepsilon_s K_B T}{2q^2 n_i} \right)^{1/2}$, intrinsic Debye length

$$F(u, u_b) = \pm \sqrt{2} \left[(u_b - u) \sinh u_b - (\cosh u_b - \cosh u_s) \right]^{1/2} \tag{3.23}$$

$F(u,u_b) < 0$ for $u > u_b$, $F(u,u_b) > 0$ for $u < u_b$

2) Evaluation of the effective space charge width (L_{sc}) from the following equation [106,107]

$$L_{sc} = L_D \frac{v_s \sqrt{\cosh u_b}}{F(u_s, u_b)} \tag{3.24}$$

where L_{sc} = effective space charge width

$$L_D = \sqrt{\frac{\varepsilon_s K_B T}{q^2 (p_b + n_p)}}$$, L_D = semiconductor extrinsic Debye length

$$v_s = \frac{V_s q}{K_B T}$$, v_s = surface potential in $\frac{K_B T}{q}$ units

V_s = surface potential in volts.

The sign convention for V_s is shown in figure 3.11. $F(u_s, u_b)$ is the same as $F(u, u_b)$ (3.23) with u replaced by u_s.

3) The average excess carrier concentration per unit volume is obtained by dividing Δn_{2d}, Δp_{2d} by L_{sc}, i.e.,

$$\Delta p_v = \frac{\Delta p_{2d}}{L_{sc}} \tag{3.25}$$

$$n_v = \frac{\Delta p_{2d}}{L_{sc}} \tag{3.26}$$

where: Δn_v and Δp_v are the average change in the electron and hole concentrations per unit volume in the space charge. The total carrier concentrations are:

$$\bar{p} = p_b + \Delta p_v \tag{3.27}$$

$$\bar{n} = n_b + \Delta n_v \tag{3.28}$$

where $\bar{p}$ and $\bar{n}$ are the total average hole and electron concentration in the space charge region. By using equations (3.19) - (3.28) $\bar{p}$, $\bar{n}$ can be calculated as a function of the surface potential (V_s).

The experiments reported in this section are mainly performed on the silicon samples with the following properties: uniformly boron doped (p type), <100>, ρ = 11-16 Ω cm ($N_A \simeq 10^{15}$ cm^{-3}).

The samples are commercially used in N MOS integrated circuit technology. The oxide is thermally grown (dry-wet-dry) with a thickness of 5000 ± 500 A^{o}. Theoretical plots of $\bar{p}$ and $\bar{n}$ as a function of surface potential are shown in figure 3.10. Even though the carrier concentration of 10^{15} cm^{-3} corresponds to $u_B = -11.1$, the value of $u_B = -12$ is used in figure 3.10 because it makes it possible to use the plots in reference [107] in order to calculate Δp_{2d} and Δn_{2d} (equations (3.19), (3.20)). The approximation is good and the error introduced is negligible. The range of surface potentials corresponding to accumulation, depletion, weak inversion and strong inversion are indicated in figure 3.10.

4) The TAV amplitude as a function of the carrier concentration is calculated using the procedure discussed in Chapter 2 (equation (2.40)). The resulting curve for SAW frequency of 110 MHz is shown in figure 2.3b (solid curve).

5) By using steps 3 and 4 the TAV amplitude as a function of the surface potential (TAV-V_s) is obtained and the result is presented in figure 3.11.

3.3.2 Dependence of V_s on the bias voltage and characterization of the interface charge density and flat band voltage, results and discussion

For TAV-V_B measurements the experimental apparatus discussed in section 3.1 is used [50]. The thermally oxidized silicon samples are placed on the interaction window (figures 3.1-3.3) and the back contact is provided by removing the oxide from the back

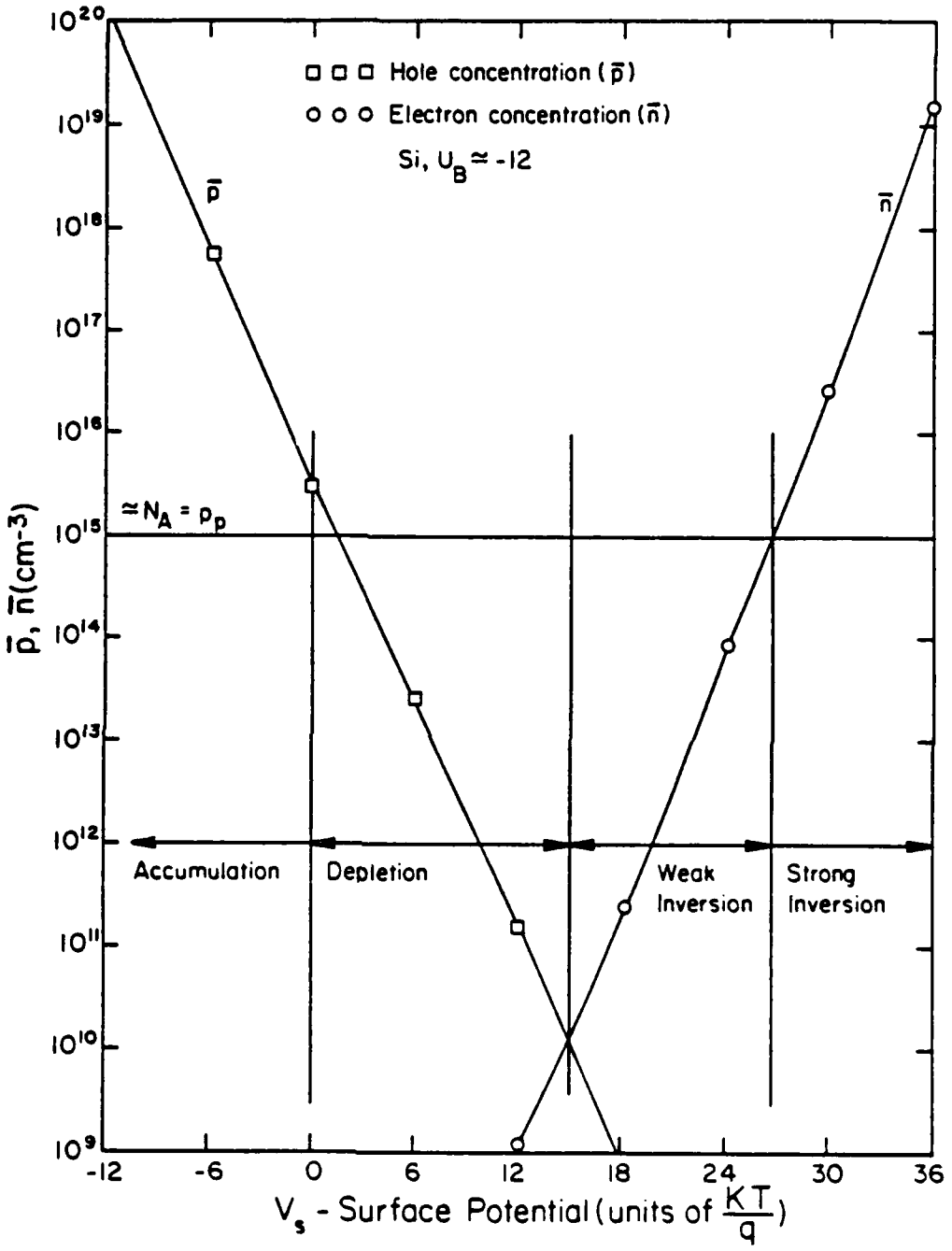

Figure 3.10 Total average electron and hole concentration in the space charge region as a function of the surface potential (Si, $N_A \simeq 10^{15}$ cm^{-3}).

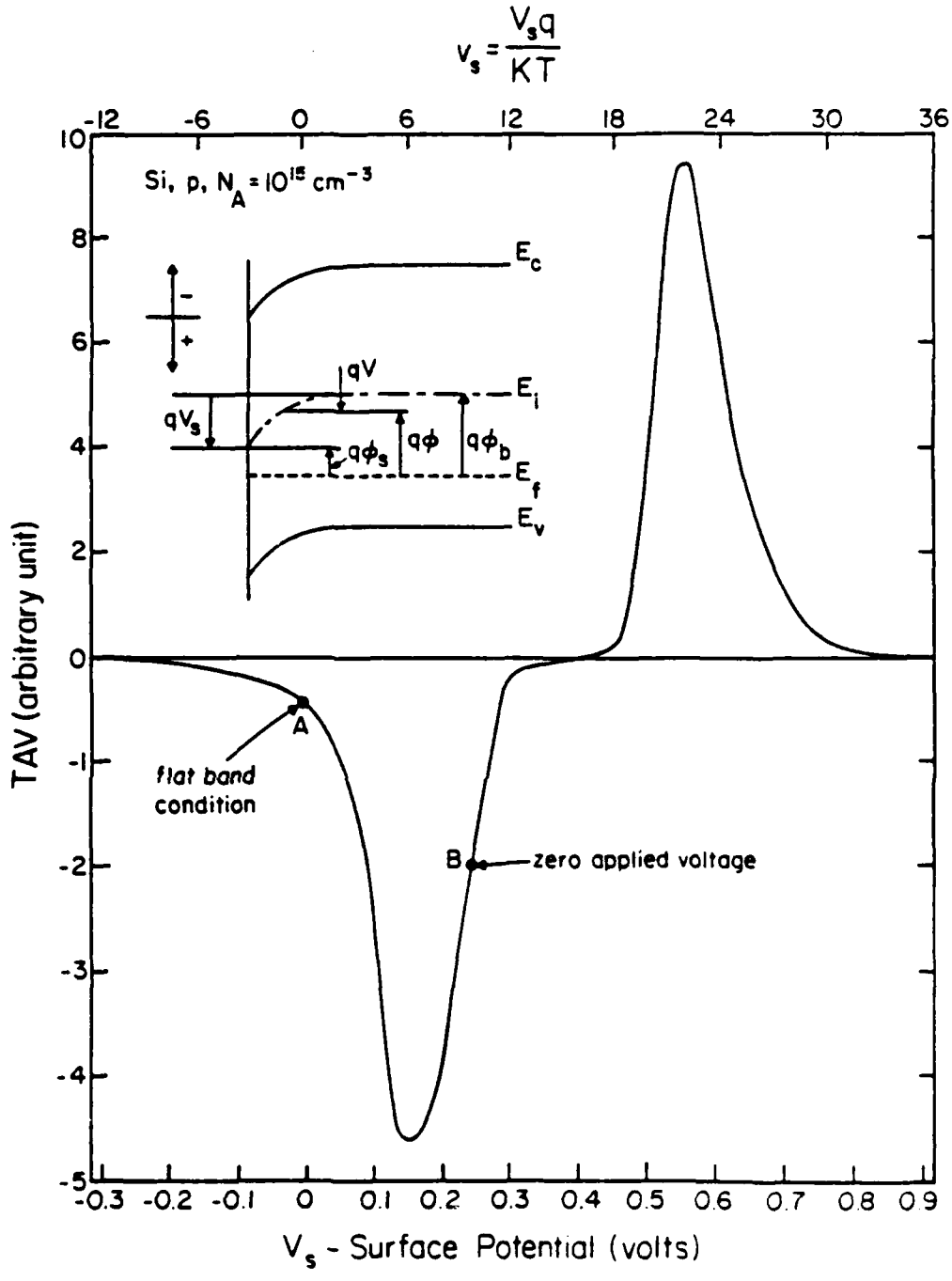

Figure 3.11 Theoretical dependence of the TAV amplitude on the surface potential for p-type silicon, ρ = 11-16 Ωcm.

surface and evaporating Aℓ with no hot step involved. The Aℓ structure on the $LiNbO_3$ surface is grounded and the bias voltage is applied to the back surface as shown in figure 3.3. The interdigital transducer is excited by 110 MHz rf pulse with 2 msec width and 10 msec period. The first harmonic of the TAV waveform which is directly proportional to the TAV amplitude is monitored by the lock in amplifier. To obtain the TAV-V_B curves, the amplitude of the TAV signal is recorded as a function of the bias voltage measured directly across the semiconductor (V_B), as the external voltage source is scanned over the desired range. In this arrangement, since the surface under study is on the ground path, the configuration is similar to the substrate biasing in MOS structures. Although there is no gate on the oxide, the voltage of the ground path with respect to the back surface bias voltage can be considered as the gate voltage. The biasing configuration is shown in figure 3.2a. The presence of the interaction window necessitates some approximation in calculating the surface potential as a function of the bias voltage. In the following, two approaches are discussed.

a) The bias voltage (opposite sign of the gate voltage in C-V) can be related to the surface potential using the following equation [50]:

$$V_B = \frac{Q_{sc}}{C_{ox}} + \frac{Q_t}{C_{ox}} - V_s - \phi_{ms} \qquad (3.29)$$

where V_B = applied bias voltage

Q_{sc} = space charge density per unit area

C_{ox} = oxide capacitance per unit area

Q_t = total interface charge density per unit area

V_s = surface potential

ϕ_{ms} = work function difference between Al and Si

Q_t can be written as:

$$Q_t = Q_f + Q_{ot} + Q_m + Q_{it} \tag{3.30}$$

where Q_f = oxide fixed charge density per unit area

Q_{ot} = oxide trapped charge density per unit area

Q_m = oxide mobile ionic charge density per unit area

Q_{it} = interface traps charge density per unit area

In the following treatments Q_{ot} and Q_m are neglected and their effect is included in Q_f (experiments are at room temperature with no stress bias). Q_{it} can be written as:

$$Q_{it} = q \int_0^{V_s} D_{it}\, dV + C \tag{3.31}$$

where D_{it} = interface trap level number density per unit area per unit energy, $cm^{-2}\ eV^{-1}$.

The constant of integration (C) is zero if it is assumed that at flat band voltage ($V_s = 0$), Q_{it} is zero. The silicon wafers used in the following experiments are specified to have low interface trap level density, (D_{it} is in the range of $10^9\ cm^{-2}\ eV^{-1}$ around the midgap) thus the effect of Q_{it} is negligible in the following discussion. The procedure that can be used to obtain D_{it} if it is not negligible, is presented later.

In this section the value that is used for C_{ox} in the calculation of V_s versus V_B from equation (3.29), corresponds to an oxide thickness of 5000 A^o. This approximation neglects the effect of the air gap present in the path of the electric field which modulates the surface potential (figure 3.2a). In order to compensate for this assumption the ϕ_{ms} term is dropped in equation (3.29) due to the absence of aluminum deposition on the area under study. Another approach which considers a thicker insulator layer (includes the air gap) and also includes ϕ_{ms} is discussed in section b.

To obtain V_s versus V_B, the value of Q_{sc} at each V_s should be calculated (step 6 in figure 3.9, section II). The following equation for Q_{sc} is used [50,107].

$$Q_{sc} = 1.3 \times 10^{-11} F(u_s, u_b) \text{ for silicon at } 300^oK \qquad (3.32)$$

where $F(u_s, u_b)$ is defined in (3.23). The plot of $|Q_{sc}|$ as a function of V_s for $N_A = 10^{15}$ cm^{-3} is shown in figure 3.12 along with the various regions. Using the above discussions, the equation (3.29) is reduced to

$$V_B = \frac{1.3 \times 10^{-11} F(u_s, u_b)}{C_{ox}} + \frac{Q_f}{C_{ox}} - V_s \qquad (3.33)$$

In the next step (step 7 in figure 3.9) equation (3.33) can be solved either numerically or by using the $|Q_{sc}|$ versus V_s plot from step 6. The former is used and the result is shown in figure 3.13. Two plots associated with N_f values of 8.5×10^{10} cm^{-2} and 7.0×10^{10} cm^{-2} ($N_f = Q_f/q$ = oxide fixed charge number density per unit area) are presented, exhibiting a constant voltage shift along the

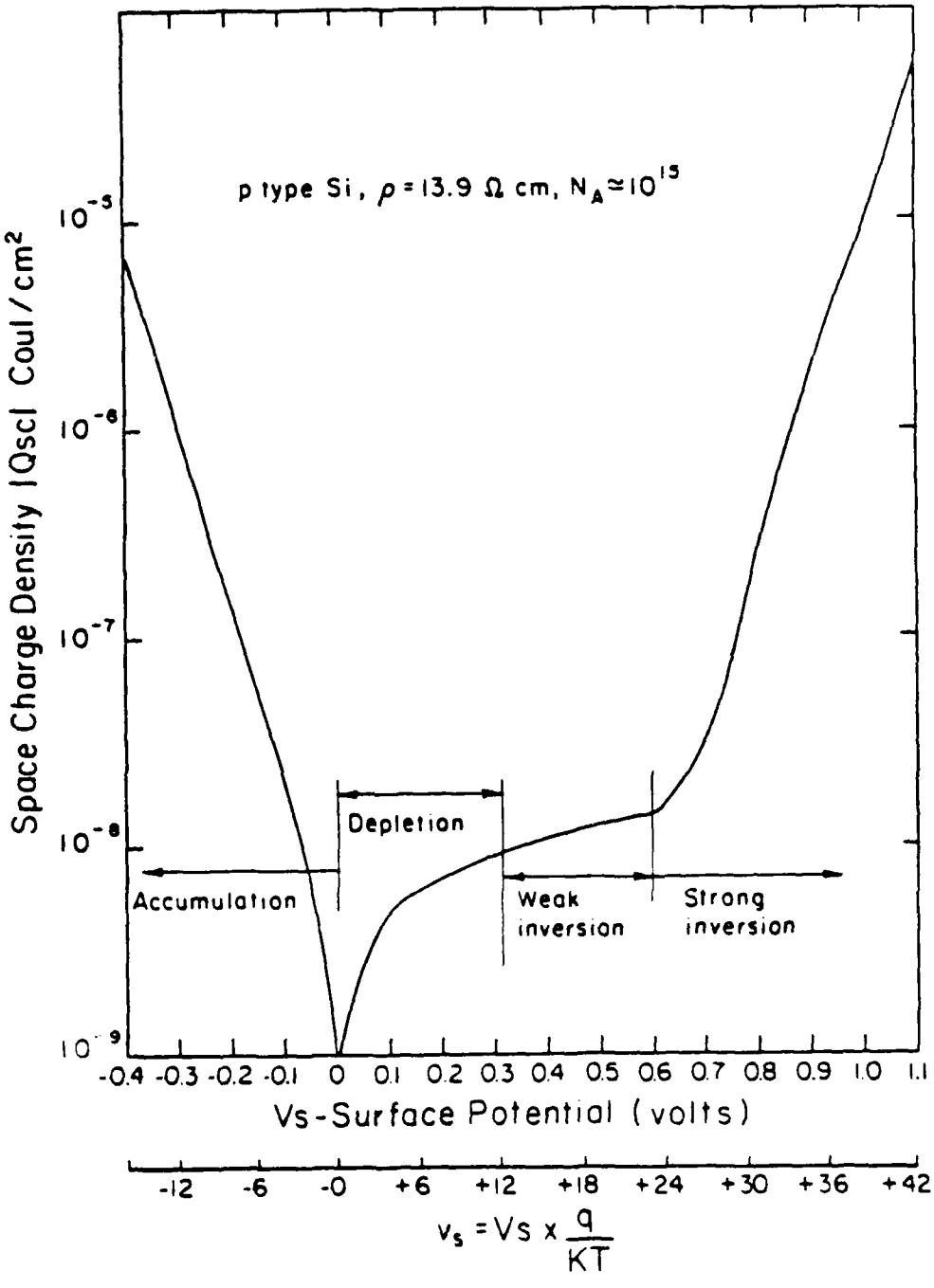

Figure 3.12 Space charge density as a function of the surface potential (Si, $N_A \simeq 10^{15}$ cm^{-3}).

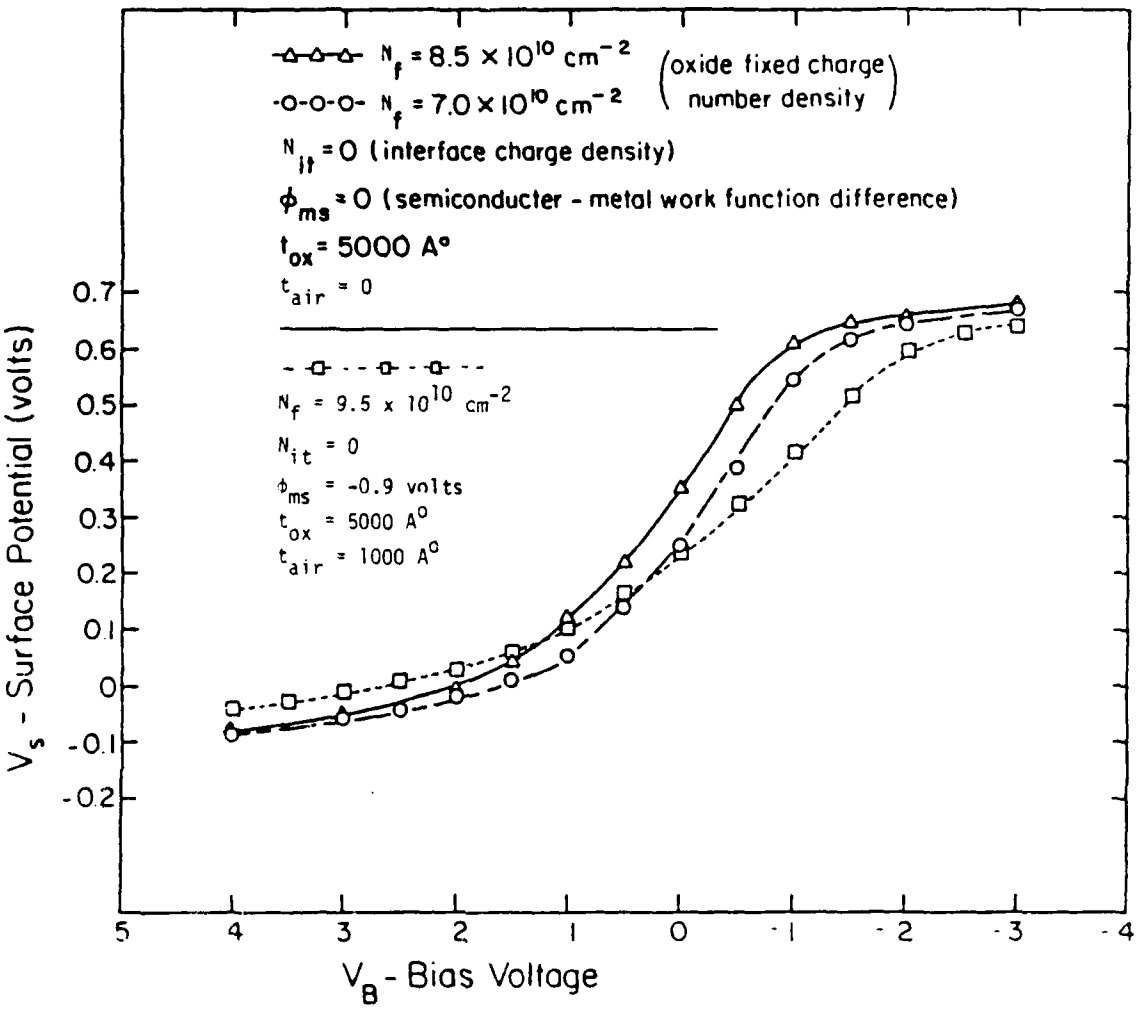

Figure 3.13 Surface potential as a function of the bias voltage for different oxide fixed charge densities and different calculation approaches (Si, $N_A = 10^{15}$ cm^{-3}).

V_B axis. The third plot (dotted curve) assumes a finite air gap and is discussed in part b. By using the plots from figures 3.11 (step 7) the theoretical TAV-V_B curves at different values of Q_f can be obtained (step 9). The value of Q_f is then chosen for the best fit between the experimental and theoretical TAV-V_B curves. Obviously, different values of Q_f only shift the theoretical TAV-V_B curve along the voltage axis. Figure 3.14 shows the experimental and theoretical TAV-V_B curves. The solid curve (plot 1) is the experimental curve. The dashed curve (plot 2) is the theoretical curve by using the above assumptions. The dotted curve (plot 3) is the theoretical curve, using the assumptions of non zero air gap and metal semiconductor work function, as discussed in part b. It should be noted again that the polarity of the bias voltage in these curves is opposite of the gate voltage applied in C-V measurements.

Considering the experimental curve (figure 3.14), at zero bias the TAV amplitude is negative indicating an average p type conductivity. A quick estimation of the surface potential at each bias voltage is possible by considering figure 3.11. The plot of the normalized TAV amplitude versus surface potential in figure 3.11 exhibits a shape (the presence of the peaks and the zero cross over) which allows the one to one correspondence between the experimental TAV-V_B curve and the theoretical TAV-V_s plot. Therefore by comparing figures 3.14 and 3.11 the surface potential of about 0.25 volts can be estimated at zero bias voltage (point B in figure 3.11). Since ϕ_b = 0.29 volts, the V_s = 0.25 volts indicates

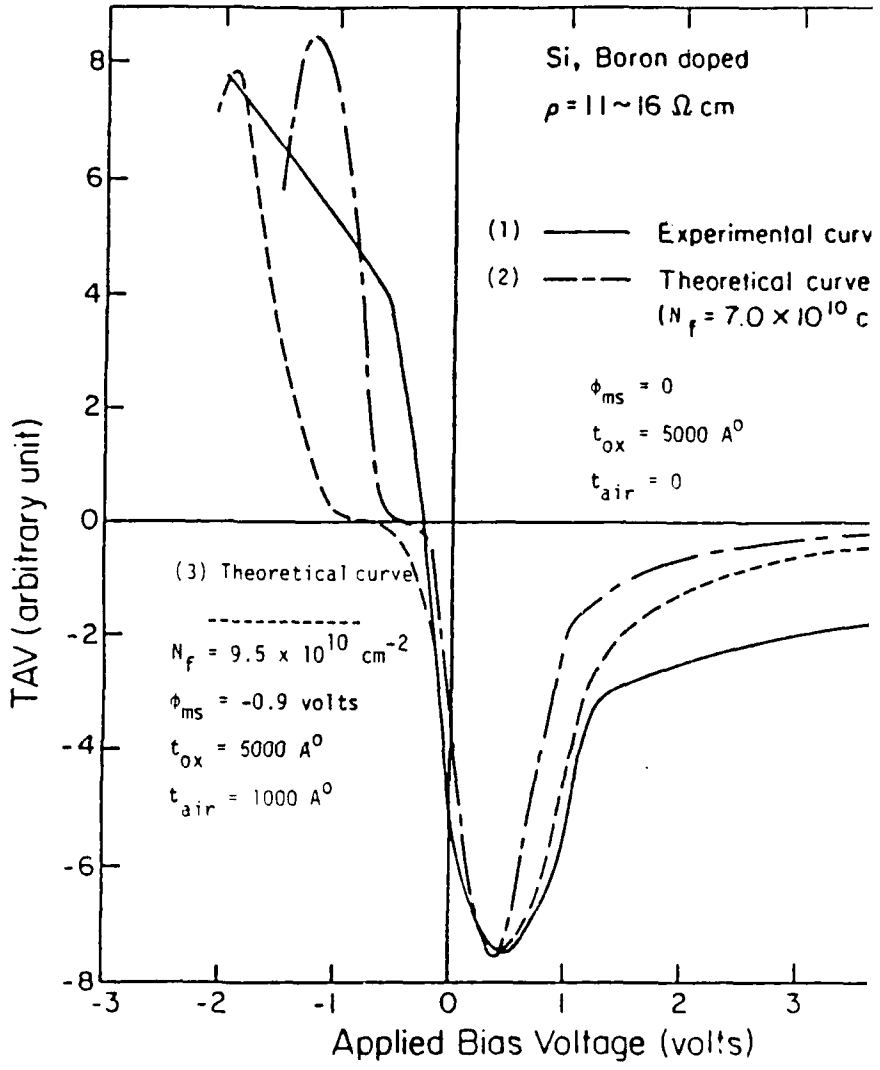

Figure 3.14 Experimental and theoretical TAV-V_B curves p type Si, ρ = 11-16 Ω cm.

the strong depletion at zero bias. By increasing the bias voltage in the positive direction the surface potention moves towards flat band (point A in figure 3.11) and accumulation. The experimental curve (figure 3.14) follows the shape of the TAV-V_s curve and after going through a minimum peak, the TAV amplitude tends to zero. By applying negative bias voltage the TAV amplitude rises sharply and goes through zero towards positive values which is the indication of a net average electron conductivity. Thus the onset of inversion can be easily estimated by the change in the TAV polarity. The experimental TAV-V_B curve is sharper than the TAV-V_s plot near the cross over region because the V_s dependence on V_B is nonlinear (figure 3.13) and the slope of the V_s - V_B curve is higher in this region. By transforming the TAV-V_s curve to the theoretical TAV-V_B curve, via V_s - V_B plot, it can be observed that indeed the TAV-V_B is sharper than TAV-V_s around the zero cross over (curve 2 in figure 3.14), but the experimental TAV-V_B is even sharper than the theoretical TAV-V_B. The reason for this effect is discussed later. As mentioned earlier, the value of Q_f is chosen for the best fit between theoretical and experimental TAV-V_B curves. This fit is provided by choosing $N_f = 7 \times 10^{10}$ cm^{-2} (corresponding to $Q_f = 1.12 \times 10^{-8}$ C/cm^2) as shown in figure 3.14, curve (2). Now in order to find the flat band voltage, equation (3.33) is considered. At flat band $Q_{sc} = 0$, $V_s = 0$ and (3.33) reduces to

$$V_{FB}(SAW) = \frac{Q_f}{C_{ox}} \qquad (3.34a)$$

It should be noted that in equation (3.34a), the effect of ϕ_{ms} is neglected. The equivalent flat band voltage in C-V measurement with aluminum gate deposited on the oxide would be

$$V_{FB}(C\text{-}V) = \frac{-Q_f}{C_{ox}} + \phi_{ms} \qquad (3.34b)$$

where a sign reversal is applied for gate voltage. The value of ϕ_{ms} for Aℓ and Si with doping concentration of 10^{15} cm^{-2} is about -0.9 volts [60]. In equation (3.34a) by using

$$Q_f = 1.12 \times 10^{-8} \text{ C/cm}^2$$

and $$C_{ox} = 6.9 \times 10^{-9} \text{ F/cm}^2 \text{ for } t_{ox} = 5000 \text{ A}^{\circ},$$

we have: $V_{FB}(SAW) \simeq 1.6$ volts and the equivalent flat band voltage for C-V is: $V_{FB}(C\text{-}V) = -1.6 - 0.9 = -2.5$ volts. For comparison the C-V plot of the aluminum gate MOS capacitor, fabricated on the similar silicon wafer (ρ = 11-16 Ω cm, boron doped, thermally oxidized) is shown in figure 3.15. It can be observed that at zero gate voltage the surface is strongly depleted. To obtain the flat band voltage, the ratio of the flat band capacitance (C_{FB}) to the oxide capacitance is obtained using the plots in reference [60]. This ratio is about 0.92 for this sample. The flat band voltage is the bias voltage at which the measured capacitance is equal to C_{FB}. Using figure 3.15 the V_{FB} of about -2.5 volts is obtained which is in very good agreement with the value obtained from the TAV measurement. The oxide thickness calculated from the accumulation capacitance is about 5300 A°. Now in order to calculate the C-V equivalent flat band voltage from the TAV measurement (equation

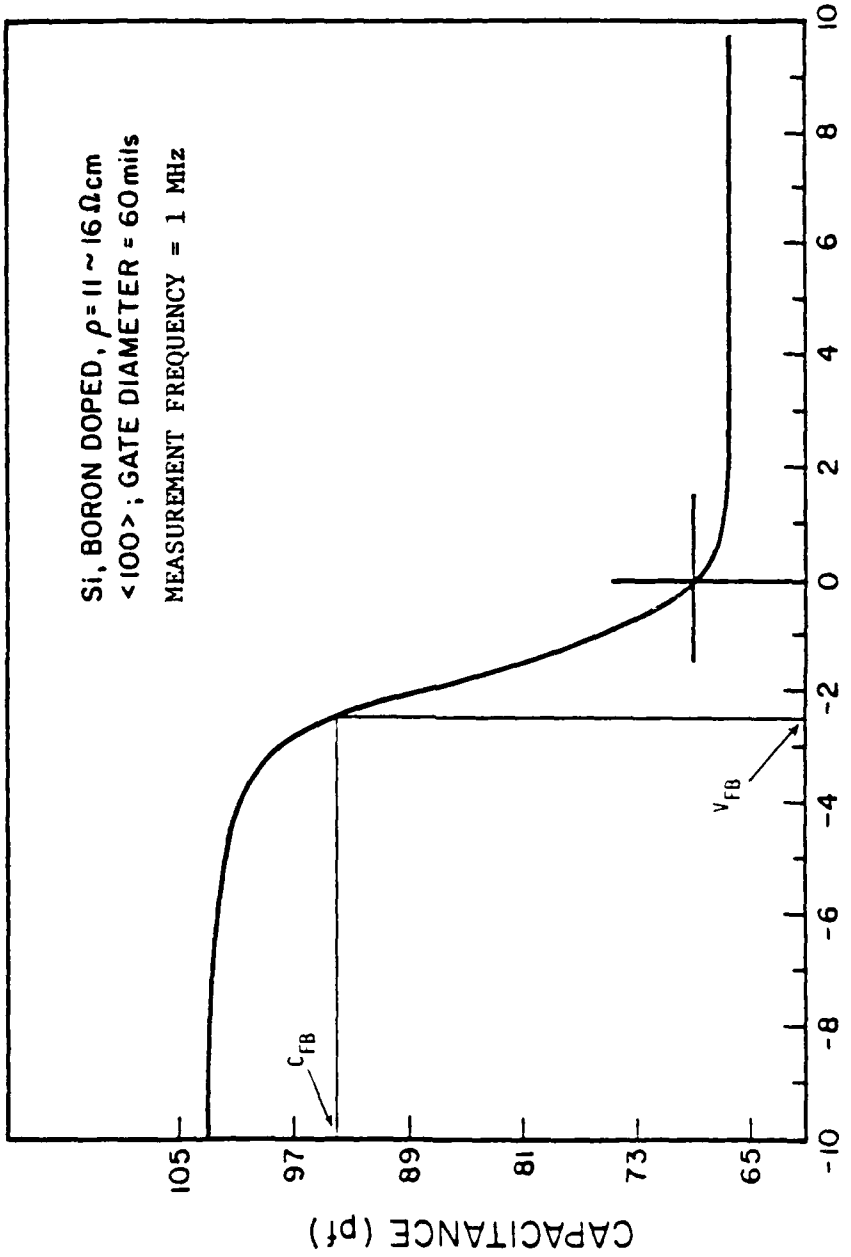

Figure 3.15 Capacitance voltage curve for the p type Si, $\rho \simeq 11\text{-}16\ \Omega$ cm ($t_{ox} \simeq 5300\ A^{o}$).

which can be on the order of ± 500 A^{o} can cause discrepancy between the theoretical and experimental curves. For thicker oxides the theoretical curve will be wider in the depletion region (better fit) due to the increase in the voltage drop across the oxide. The second dissimilarity between theoretical and experimental TAV-V_B curves which is the faster approach of the theoretical curve to zero in the accumulation region can also be due to the above phenomena.

The deviations of the experimental curve from theory in the inversion region (TAV positive) and the possible causes are as follows: 1) The slope of the experimental TAV curve in passing through zero is sharper than the theoretical curve and the cross over point is slightly closer to zero bias voltage. This effect can be caused by a source of minority carriers which provides the carriers at a higher magnitude than what is predicted by equation (3.29). The minority carrier source can be due to the reduction of the oxide thickness below its estimated value (or even a puncture in the oxide) at some points of the wafer surface which is in contact with the ground path. If these sources are closer to the interaction window (figure 3.2a) than a minority carrier diffusion length (which can be on the order of tenths of millimeter), then the carriers can diffuse to the interaction window and contribute to the TAV amplitude. This effect is much more pronounced around the cross over point because the TAV amplitude is very sensitive to the free carrier concentration in this region. 2) In the positive TAV region the theoretical TAV-V_B curve goes through a peak

as the minority carrier concentration increases. The reason that the experimental curve does not show the peak, is due to the voltage scan rate which is about 70 mV/sec in this experiment. If the minority carrier response time is very long (which can be on the order of 100 seconds as will be seen later), then the minority carrier concentration will not be at equilibrium with the applied bias voltage. This effect is experimentally verified, and at smaller scan rates (on the order of 10 mV/sec) the peak can be observed.

To show the applicability of the TAV-V technique for high resistivity samples, a p type silicon substrate with resistivity of about 2800 Ωcm was tested. The result is shown in figure 3.16. From the TAV-V_B curve it can be deduced that the surface is close to flat band at zero bias voltage. The surface potential at zero bias is estimated by comparing the TAV-V_B curve to a plot similar to the one presented in figure 3.11.

b) In this part the dependence of V_s on V_B is considered using the following assumptions. 1) the air gap which is present in the path of the bias field contributes to the total capacitance (C_{ta}). Thus in equation (3.29) C_{ox} should be replaced by

$$C_{ta} = \frac{C_{ox}\, C_{air}}{C_{ox} + C_{air}} \tag{3.35}$$

where C_{air} is an estimate of the capacitance due to the air gap which is in series with oxide capacitance. If the arrangement in figure 3.2c is used, an estimate of C_{air} is simply

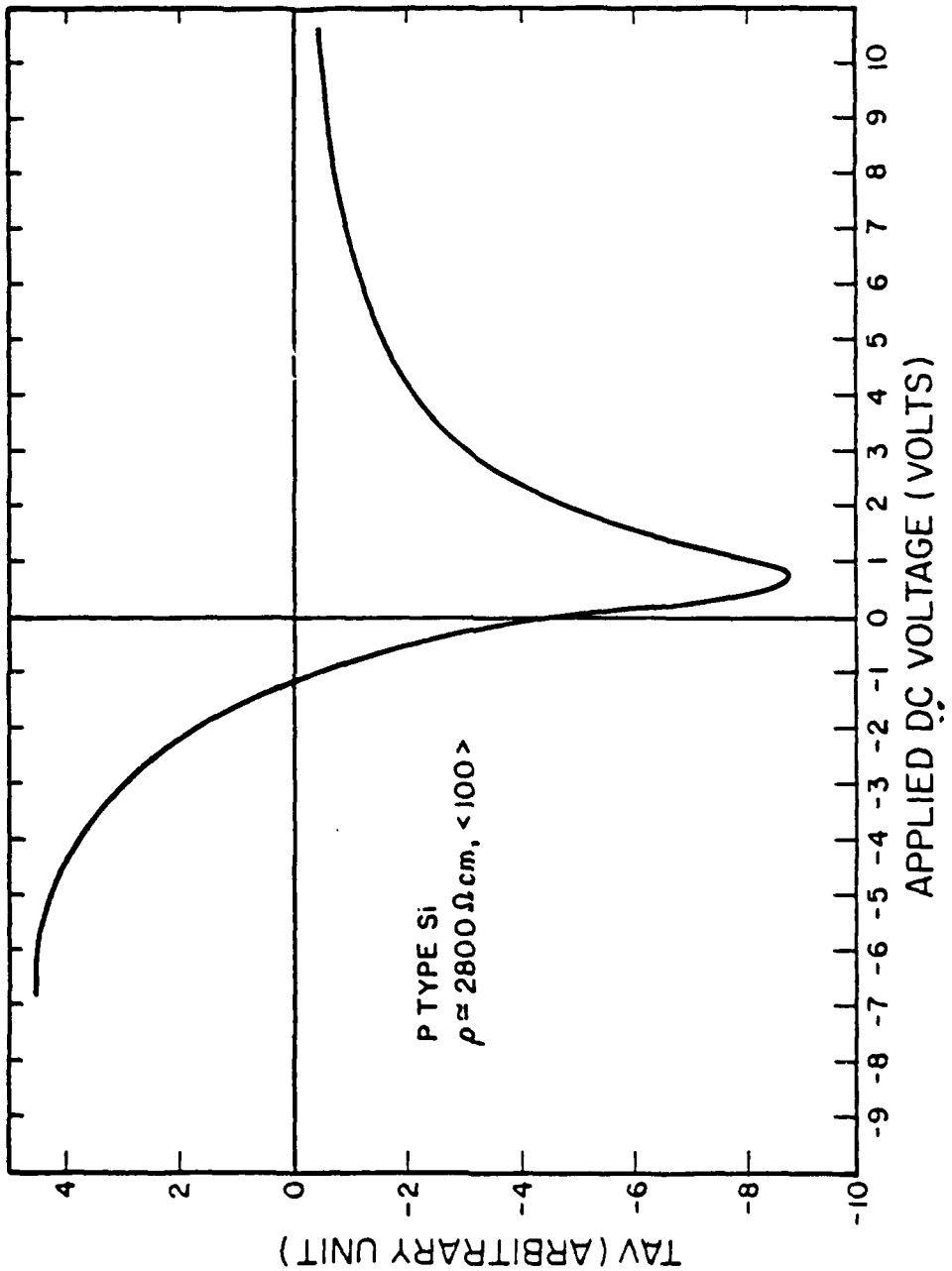

Figure 3.16 Experimental TAV-V_B curve for p type Si, $\rho \simeq 2800\,\Omega$ cm.

$$C_{air} = \frac{\varepsilon_o}{t_a - t_w}$$ where ε_o = permitivity of the free space, and t_a, t_w are defined in figure 3.2c.

The value of the air gap capacitance affects the width of the theoretical TAV-V_B curve. Thus it can be adjusted for any delay line structure (figures 3.2a,b) in order to provide the best fit for a known sample and then be used as a constant. In the following experiments the airgap thickness of 0.1 μm is used. The ϕ_{ms} is not neglected in this case and the value of -0.9 volts is used for Aℓ and Si. Equation (3.29) is used in the following form:

$$V_B = \frac{Q_{sc}}{C_{ta}} + \frac{Q_f}{C_{ta}} - V_s + 0.9 \qquad (3.36)$$

where C_{ta} is defined in (3.35) and Q_f is chosen for the best match between theoretical and experimental curves. The V_s versus V_B plot for this case is shown in figure 3.13 (dotted curve). It can be observed that the slope of the curve is smaller than the previous case (airgap = 0) due to the voltage drop across the airgap. The theoretical TAV-V_B curve is obtained by using figures 3.13 and 3.11. The result is shown as the dotted curve in figure 3.14 (curve 3). Here also different values of Q_f only shift the theoretical TAV-V_B curve along the voltage axis. The $Q_f = 1.5 \times 10^{-8}$ c/cm^2 corresponding to $N_f = 9.5 \times 10^{10}$ cm^{-2} provides the best fit. Figure 3.14 shows that the theoretical curve in this case is indeed closer to experiment in the depletion region. However, in the inversion region there is a larger difference between theory and experiment. The reason is the same as discussed in part a), except that the

minority carrier sources cause a stronger deviation in this case due to a higher voltage drop across the insulator layer. The C-V equivalent flat band voltage is:

$$V_{FB}(C\text{-}V) = -\left(\frac{Q_f}{C_{ox}} - \phi_{ms}\right) = -\left(\frac{1.5 \times 10^{-8}}{6.5 \times 10^{-9}} + .9\right) \simeq -3.2 \text{ volts}$$

The estimated value from the C-V curve (figure 3.15) is -2.5 volts which is closer to the value obtained in part a (-2.6 volts). In the above cases, instead of choosing the Q_f and then plotting the TAV-V_B, it is possible to plot the TAV-V_B with zero Q_f (ideal condition) and then estimate the V_{FB} and Q_f by comparing the flat band conditions (same as C-V). However, the former procedure provides a better estimation and physical insight.

c) In both parts a and b, the effect of interface states in distorting the V_s versus V_B curve (stretch out effect) is neglected. If the interface trap level density (D_{it}) is larger than 10^{10} cm^{-2} eV^{-1}, then their effect cannot be neglected. In this case a method similar to high frequency C-V [113] can be adapted for the TAV-V measurements.

The block diagram of this scheme is shown in figure 3.17. The following steps should be taken: 1) Obtain the experimental TAV-V_B plot. 2) The theoretical TAV-V_s should be calculated as discussed earlier (figure 3.11). 3) Both TAV-V_s and TAV-V_B are normalized to exhibit the same peak values. Then a plot of the V_s versus experimental V_B can be obtained by recording the V_s and V_B values at each TAV amplitude. It should be noted that this plot

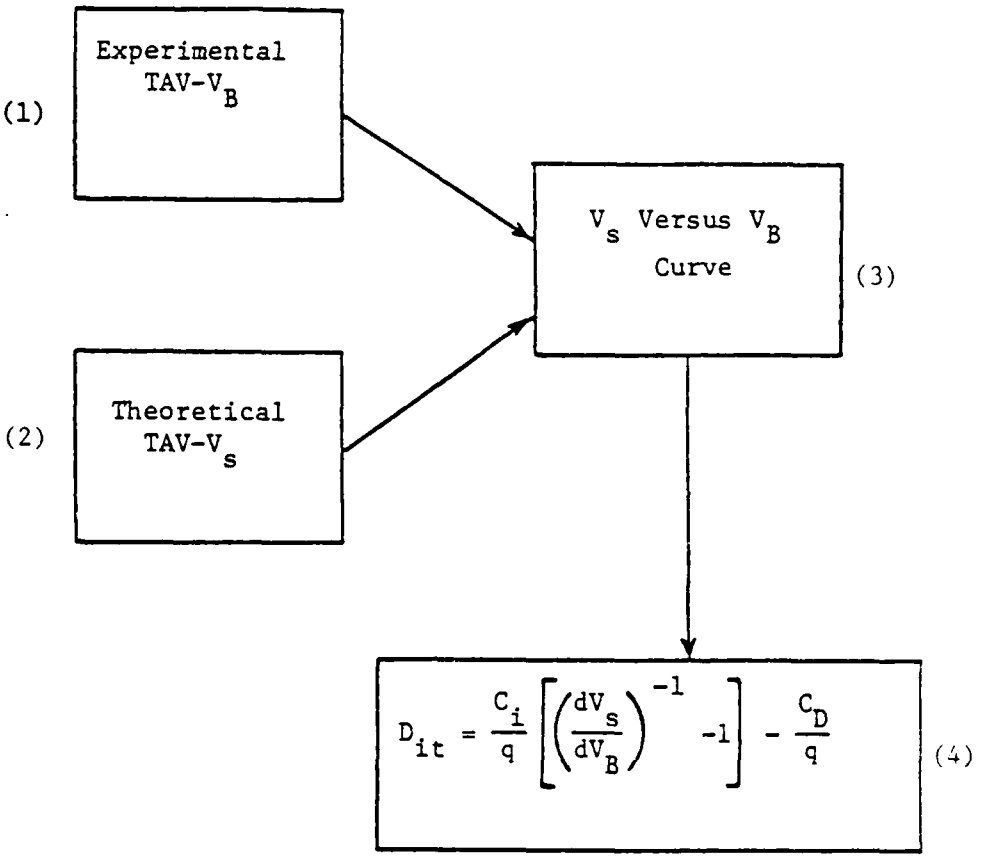

Figure 3.17 Block diagram for the interface trap level density determination.

is different from the theoretical plots obtained previously (figure 3.13) due to the interface states stretch out effect. The interface trap level density can then be obtained from the slope of the V_s-V_B curve by using the following equation [58].

$$D_{it} = \frac{C_{ta}}{q}\left[\left(\frac{dV_s}{dV_B}\right)^{-1} - 1\right] - \frac{C_d}{q} \qquad (3.37)$$

where C_d = space charge capacitance per unit area

and $$C_d = \frac{\varepsilon_s}{L_{sc}} \qquad (3.38)$$

where L_{sc} = effective space charge width (equation (3.24)).

In another method the pulsed bias measurements can be used where the interface traps do not respond to the bias voltage. By comparing the data from the pulsed bias and slowly varying ramp measurements, the information about the D_{it} can be extracted.

Summary:

In this section the feasibility of the TAV-V technique for quantitative measurements of the interface charge density and flat band voltage is demonstrated. The comparison of the experimental TAV-V_B plot and the TAV-V_s curve (obtained in section 3.3.1) provides a fast and nondestructive means to estimate the surface potential at any bias voltage. This method can be used as a fast diagnostic procedure in the production lines. To obtain the flat band voltage the theoretical TAV-V_B is obtained. To do so the TAV-V_s is transformed to the TAV-V_B via the V_s versus V_B plot.

Determination of V_s-V_B is done using two different sets of assumptions (parts a and b). These assumptions can be used as good first order approximations in evaluating the oxide fixed charge (Q_f) and flat band voltage. The validity of the assumptions are checked by comparing the flat band voltages with the C-V measured value. The results indicate a very good agreement for part a (V_{FB} - -2.6 volts as compared to -2.5 volts from the C-V measurements) and a reasonable value (V_{FB} = -3.2 volts) for part b. The assumptions in part b which include the airgap effect are physically more accurate and the shape of the theoretical TAV-V_B curve is closer to the experimental one in the depletion region. In both parts the effect of interface traps are neglected. The recipe to determine the interface trap level density (D_{it}) for the samples with high trap density is presented in part c.

3.4 TAV Transient Measurements and the Estimation of Carrier Lifetime and Surface Generation Velocity

Increasing levels of integration and larger chip area of VLSI circuits demand a lower density of crystal defects and impurity contaminations. These imperfections reduce the yield of the fabricated chips by introducing flaws in the integrated circuits. Therefore the chip area is limited by the defect density. The crystal defects and contaminations (most importantly metallic impurities such as transition group elements) produce deep level traps within the semiconductor bandgap. These levels act as generation-recombination (g-r) and trapping centers within the

semiconductor bulk and at the semiconductor interface. In the indirect gap semiconductors such as silicon where the band to band transition has a small probability, these levels determine the carrier recombination lifetime. In the dark condition, the carrier generation process also proceeds dominantly via these levels for both direct and indirect gap semiconductors. Therefore to monitor the defect density in the semiconductor bulk and interface, the lifetime measurements can be used. The fundamental parameters associated with traps and kinetics of the generation-recombination process are: 1) the capture probability rate for electrons and holes (c_n, c_p), 2) the emission probability rate for electrons and holes (e_n, e_p), 3) the energy of the trap levels within the gandgap. The generation and recombination lifetimes are phenomenological parameters [65] which are not only a function of the above fundamental parameters, but also, a function of the trap level density. Generation lifetime corresponds to the generation process in the region with a deficit of carriers below the equilibrium value ($np < n_i^2$) whereas recombination lifetime applies when excess carriers are present ($np > n_i^2$).

There are several methods for carrier lifetime determination such as photo-conductivity decay [123], reverse recovery measurement [125], impedance measurements [58] and transient capacitance measurements [64-70]. The last two techniques are extensively used for silicon bulk and interface characterization. The impedance measurement of MIS structures is a small signal, quasi-steady state

technique which is more accurate and better understood [58]. It involves more complicated measurements (compared to C-t measurement) at different frequencies, temperatures and bias voltages. It can provide the information about the capture rates and trap level density as a function of energy within the band gap. The transient capacitance methods are large signal, nonequilibrium processes where the rate of change of the depletion layer width after the application of a bias voltage is measured (usually the abrupt space charge edge (ASCE) approximation is considered). The measurements are applied to Schottky barrier, p-n junction and MIS structures. These methods can be divided into two categories: 1) the measurements where the final state does not include the formation of an inversion layer. In these cases, by using proper biasing arrangement, the rate equations can be related to the trapped charges in the bulk deep levels. The shape of the transient signal is close to an exponential with a time constant which is approximately the inverse of the sum of the electron and hole emission rates [63,64]. The information about the trap density is not included in the transient time constant, rather it can be obtained from the change in the measured capacitance at $t=0^{+}$ (the beginning of the applied bias voltage). Deep level transient spectroscopy (DLTS) [66] is an example of this technique. 2) the measurements where the final state includes the formation of an inversion layer [67,68]. In this case which is only applicable to MIS structures, the rate equation is developed for the minority carrier density in the

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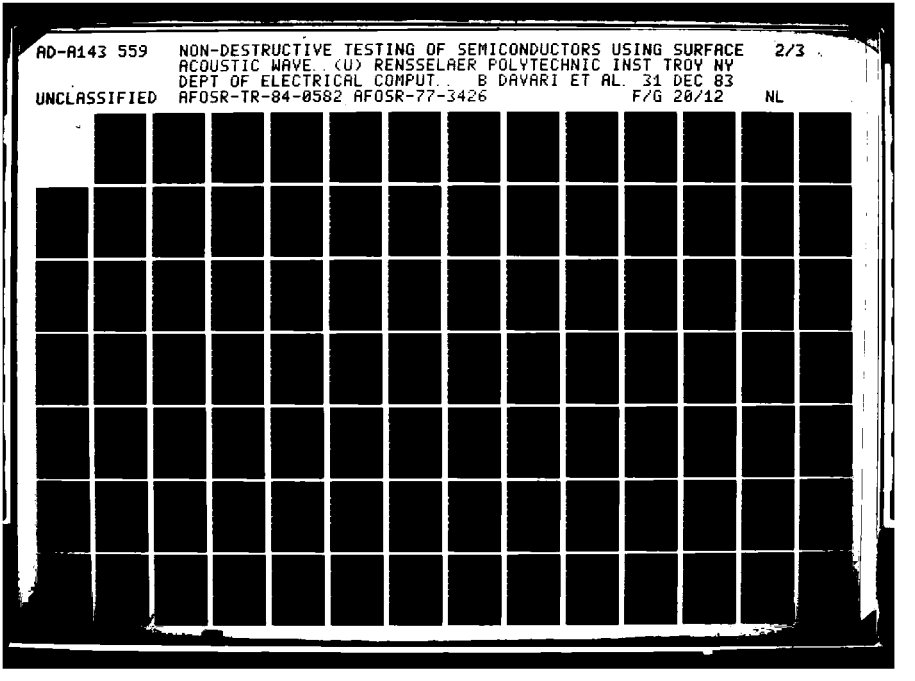
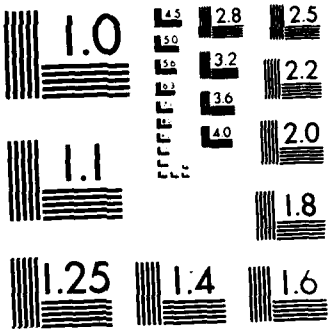




inversion layer. The form of the transient capacitance versus time (C-t) is not necessarily exponential. The mathematical manipulation of the (C-t) curve provides an approximation of the generation lifetime (τ_g) and possibly the surface generation velocity (S_g) [67,68, 126]. The approximations are valid in a limited interval of the transient response time and should be carefully examined [127]. The time scale of the C-t transient is typically several orders of magnitude larger than the generation lifetime. The amplification factor (multiplier of the generation lifetime) is on the order of $\frac{N_A}{n_i}$ (N_A is the dopant concentration) if the depletion approximation is valid ($np << n_i^2$). As mentioned earlier the measured τ_g includes both the effects of capture rate and the trap density, i.e., higher trap density results in a lower lifetime. The measurement does not uniquely determine the defect density and capture probability rate, unless performed at different temperatures. This method can be used for comparison of the defect density in samples with similar substrate properties which have undergone different fabrication processes.

In this section, the application of the TAV transient time constant measurements in the estimation of τ_g and S_g is presented. First the TAV transient waveform and the circuit requirements are discussed, followed by the theoretical treatment, relating the measured time constant to τ_g. The fabrication of p-n junction, Schottky barrier or MIS structures on the surface under study is not necessary. The theoretical treatment considers the development

of the TAV signal through an insulator layer which can be either a deposited insulator (e.g., an oxide) or the semiconductor depletion region. This treatment which effectively considers an MIS structure does not necessitate the fabrication of the MIS, due to the arrangement used for the signal detection and bias application (figures 3.1, 3.2) as discussed in earlier sections. The TAV is considered as a perturbation, added to the depleting bias voltage and different mechanisms contributing to the transient process are discussed. At different ranges of the bias voltage, the dominant mechanism can vary from bulk g-r process to surface g-r and trapping. The experimental results obtained for silicon wafers are presented in the next chapter.

3.4.1 The TAV Transient Waveform and the Circuit Requirements

In Chapter 2 the dependence of the TAV amplitude on the free carrier concentration is worked out. In the calculations, a steady state condition was assumed where the total current density in the semiconductor was zero. In this section the transition of the TAV amplitude between zero and its steady state value is considered. During this transition a small displacement current passes through the semiconductor and the required charge polarization which supports the TAV amplitude will be established. For a qualitative discussion, figure 3.18 is considered. As discussed earlier, the nonlinear interaction of the probing electric field and the near surface free carriers causes a depletion within the interaction

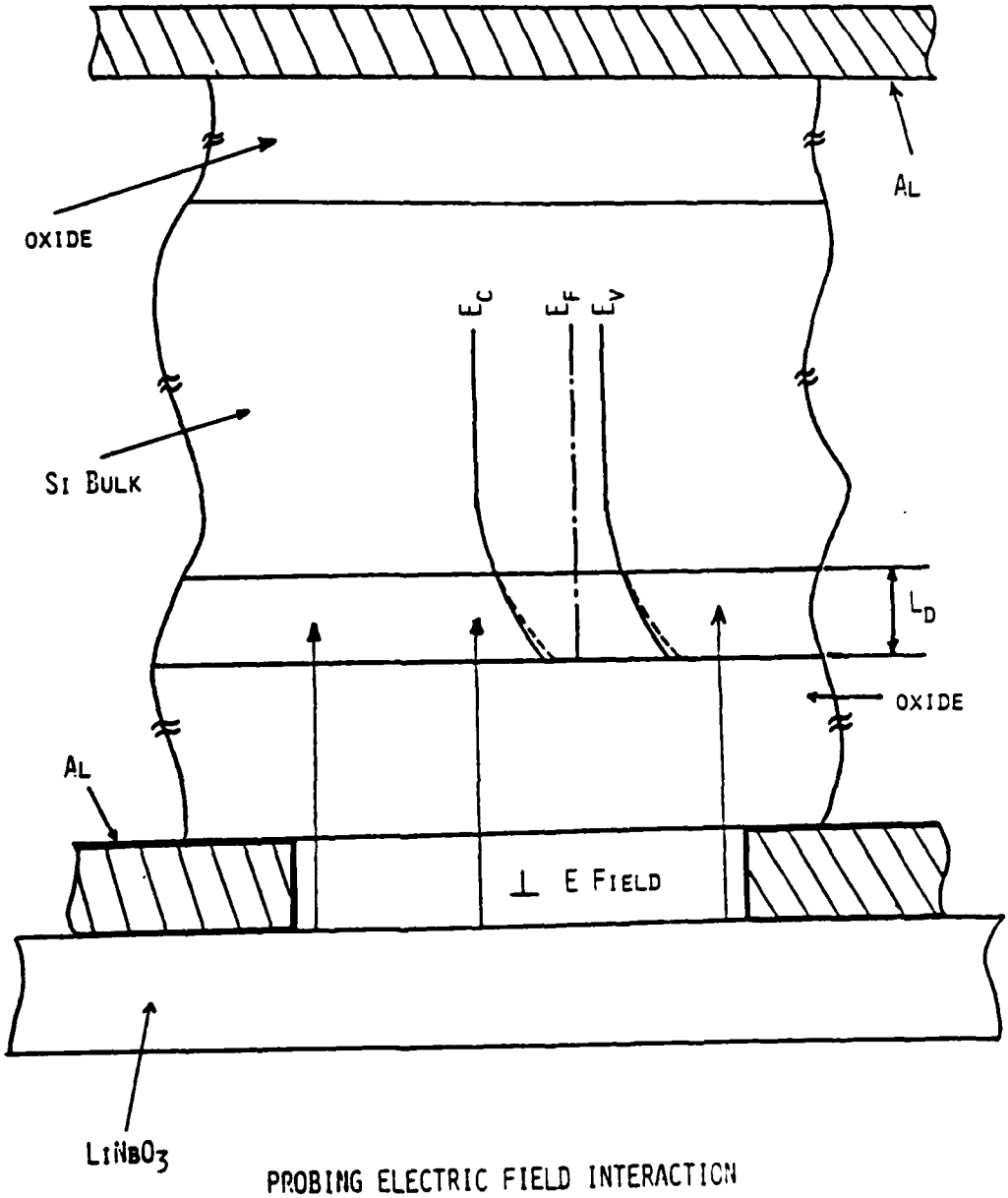


Figure 3.18 Interaction between the rf probing field and the semiconductor free carriers.

region (noted by L_D in figure 3.18). Therefore the carrier concentration is modulated, the minority carrier concentration increases and majority carrier density decreases. In this argument it is considered that the surface is depleted by the bias voltage prior to the application of the rf pulse. Therefore the contributions of both majority and minority carriers are important in developing the TAV. After the application of the rf probing field the minority carriers can be provided by the following mechanisms: 1) diffusion of minority carriers from the bulk to the interaction region, 2) generation via the bulk traps, present within the interaction region, 3) generation via the interface traps at the silicon surface. Majority carriers are mainly swept out under the influence of the electric field in the interaction region. It is assumed that the generation rate of majority and minority carriers via trap levels are equal in the interaction region (i.e., the trap level charge occupancy is time independent). The minority carrier diffusion current from the bulk can be neglected at room temperature. Therefore the mechanisms involved in establishing the new steady state minority carrier concentration are the g-r processes via bulk deep levels and interface states. The faster process dominates the transient response at any bias voltage. Therefore the time constant associated with the TAV transient (τ_{eff}) is related to the carrier lifetimes. For example, it will be shown that at near midgap bias (the bias at which the Fermi level is close to the midgap at the surface) the bulk generation can be dominant (if the substrate is

p type and trap energy level is below E_i in the bulk). In this case τ_{eff} is directly proportional to τ_g with an amplification factor (the parameter which is multiplied by τ_g) which will be determined in the next section. The depletion approximation cannot be used in this case due to the small magnitude of the TAV signal.

The basic experimental apparatus is shown in figure 3.19 which is very similar to figure 3.3. The arrangement for the bias application is not shown in figure 3.19, but it is the same as figure 3.3. To obtain the plot of the τ_{eff} as a function of the bias voltage, automatically, the lock in amplifier in figure 3.3 is replaced by a computer. The detected signal truly reflects the TAV transients only if the circuit loading effect is negligible. TAV waveforms and the rf pulse are shown in figure 3.20. For an ideal measurement the TAV reaches its steady state value with the time constant τ_{eff} and then remains constant (figure 3.20b). Experimentally the measured TAV falls off with the time constant τ_c due to the capacitive coupling and amplifier loading (figure 3.20c). The coupling capacitances have a minimum value in the range of 50 pf. By using a high input impedance amplifier the value of τ_c (which is the upper limit of measurement) can be on the order of a fraction of a second which is appreciably higher than τ_{eff} (on the order of 100 μsec). The lower limit of the τ_{eff} measurement is determined by the transition time of the surface acoustic wave across the interaction window which is about 0.5 μsec. The lower limit of τ_g can be appreciably shorter due to the amplification factor, relating

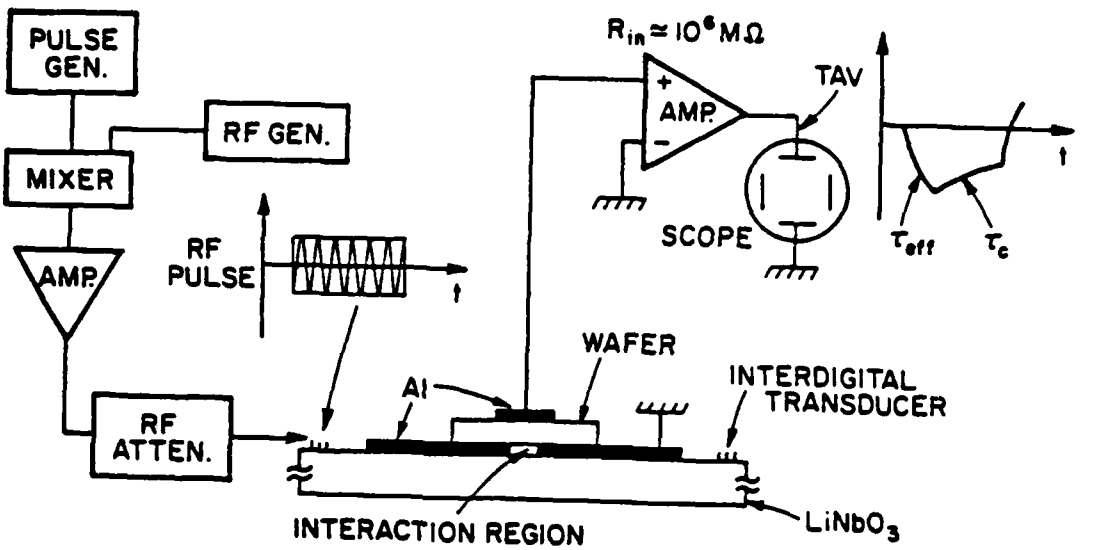


Figure 3.19 Experimental apparatus for the TAV transient time constant measurements.

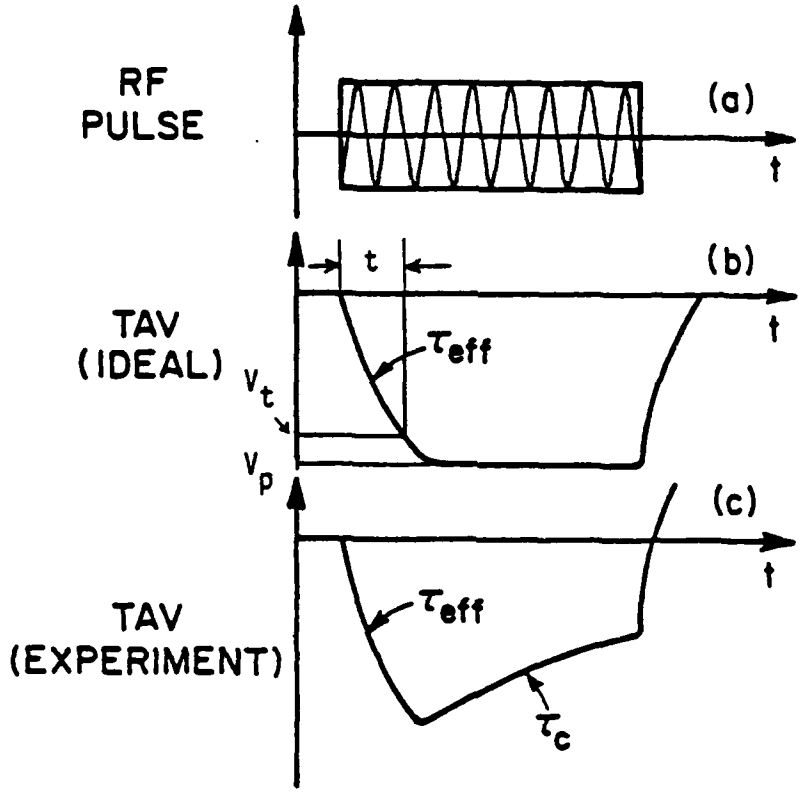


Figure 3.20 TAV waveform in the transient time constant measurement.

τ_{eff} and τ_g. Considering the time constant associated with the external circuit (τ_c), the TAV signal has the following form:

$$V_t = \frac{\dot{V}_p \tau_c}{\tau_c - \tau_{eff}} \left(e^{-t/\tau_c} - e^{-t/\tau_{eff}} \right) \qquad (3.39)$$

where

V_t = transient TAV amplitude

V_p = the TAV amplitude at steady state as calculated in Chapter 2, equation (2.40).

In order to extract the value of τ_{eff} from the TAV waveform directly, the value of τ_c should be much larger than τ_{eff}. An experimental TAV waveform for an oxidized silicon wafer (p type, ρ = 11-16 Ωcm) is shown in figure 3.4 along with the corresponding rf pulse.

3.4.2 Qualitative Discussion of the TAV Transient Response

In this section the effects of generation lifetime and surface generation velocity on the measured TAV time constant (τ_{eff}) are discussed. The influence of these parameters on τ_{eff} varies, depending on the surface potential at different bias voltages. The effect of surface potentials on the transient process is considered as follows (figure 3.21).

A) From flatband to near midgap the majority carriers dominate the transient response. The effect of interface traps is stronger than the bulk traps. In this case, interface traps do not have to respond as g-r centers. The communciation of the interface

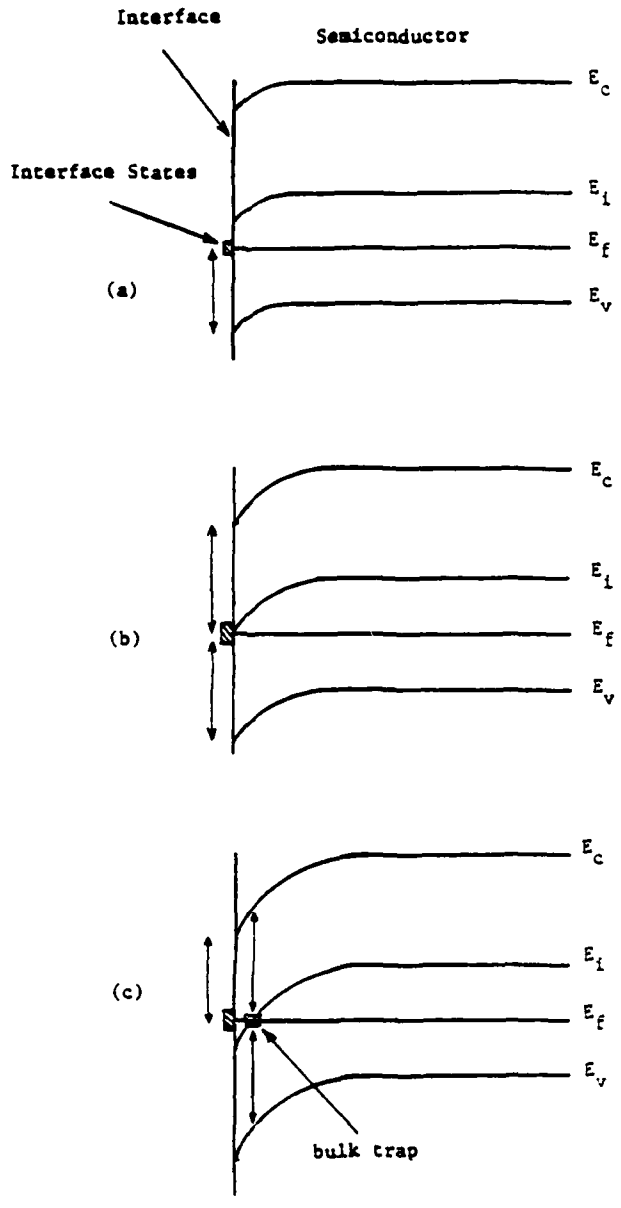


Figure 3.21 The effect of the surface potential on the interface and bulk generation recombination processes.

(a) from accumulation to near flat band
(b) near midgap
(c) from midgap to inversion

traps with only the majority carrier band is sufficient for establishing the equilibrium (figure 3.21a). The reasons are: first the transient response is mainly due to the majority carriers, and second the majority carrier drift current is dominant in the quasi neutral region. In this regime the TAV transient is fast and mainly governed by the interface traps. At any given bias only the traps within a few $\frac{K_B T}{q}$ around the Fermi level contribute to the transient response. The reason is that, in this range the trap occupancy can be changed effectively by a small band bending. On the other hand, the traps further away from E_f are either nearly full or empty and they cannot be efficient in capture and emission of carriers.

B) At surface potentials near midgap both the majority and minority carriers are important in establishing the equilibrium. In this case the trap levels which are efficient generation-recombination centers contribute strongly to the transient response (figure 3.21b). The requirements for an efficient g-r center are: 1) It should be within a few $\frac{K_B T}{q}$ around the Fermi level as discussed in part A. 2) It should be near the midgap in order to exhibit an almost equal electron and hole capture and emission rates. For example the emission rates of electrons and holes are exponentially dependent on the energy difference between the trap level and the conduction band and the valence band respectively. Therefore to obtain a nearly equal hole and electron emission rate, the trap level should be close to the midgap (assuming an almost equal

electron and hole capture cross sections). In the following discussions the trap level (E_T) is considered to be at the midgap (E_i). By increasing the depleting bias voltage towards weak inversion the g-r centers at the interface pass through the E_f before the g-r centers in the bulk (figure 3.21b). Thus a surface potential exists, at which the g-r process through the interface traps maximizes and dominates the transient response. In general, the bulk and interface effects are not clearly separated in this range of bia voltages because they can both contribute to the g-r proce

C) By changing the surface potential towards we inversion the effectiveness of the g-r centers at the interface is drastically reduced (figure 3.21c). At strong inversion the interface traps which are close to E_f cannot be near E_i. Therefore they can only communicate with the minority carrier band and cannot be efficient g-r centers. The interaction of the interface states with only the minority carrier band does not influence the transient response (as opposed to the interaction with only the minority carrier band), because the current in the quasi neutral region is almost entirely due to the drift current of the majority carriers. Therefore at bias voltages, which change the surface potential from midgap towards inversion, the effect of bulk traps near E_i (g-r centers) become increasingly important (figure 3.21c). In strong inversion the bulk g-r centers dominate the transient response.

In the TAV measurements, τ_{eff} can be obtained as a function of the bias voltage as will be shown in the next chapter. The

approximate separation of the bulk and surface effects can be obtained by lifetime measurements in the depletion and near inversion conditions. From flat band to weak depletion the interface effects dominate the transient response. In near inversion, E_i at the surface is almost equal to or slightly below E_f (p type substrate), but the average conductivity in the space charge region is still p type. In this case the TAV time constant is assumed to be only a function of the bulk generation lifetime as the interface effects are reduced. By moving towards strong inversion the average conductivity becomes n type and the TAV polarity changes. Under this condition the TAV time constant is a function of the bulk recombination lifetime. The reason is that the nonlinear interaction of the rf probing field and the free carriers tends to reduce the minority carrier concentration. Although at strong inversion the interface effects are almost completely quenched (part c), this regime is not used extensively in TAV measurements due to the smaller signal to noise ratio.

3.4.3 Theoretical Development of the TAV Transient Response

In this section the theoretical formulation governing the TAV transient response is developed. An approximate relationship between the measured TAV lifetime and generation lifetime is then worked out. At first it is assumed that at the chosen bias voltage the effects of interface states are negligible. The interface dominant case is considered next. The semiconductor band diagram is shown in figure 3.22. The bulk trap energy level is at E_T.

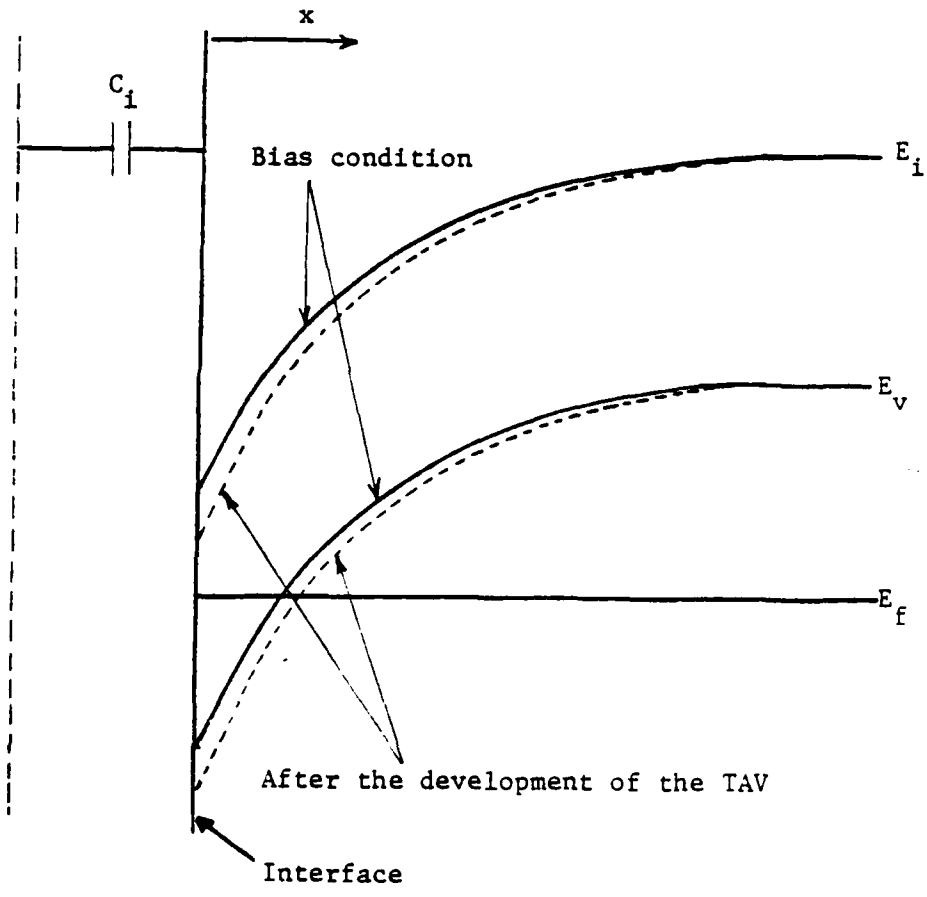


Figure 3.22 Near surface band diagram, under depleting bias voltage (before and after the TAV development).

There might be an insulator with capacitance C_i on the semiconductor surface. TAV is considered as a perturbation added to the bias voltage which produces the average band bending as shown by the broken lines. During the TAV transient, a displacement current passes through the semiconductor. The rate equation can be obtained by equating this current to the generation current within the non-equilibrium volume where $np < n_i^2$ during the transient. The following equations are considered:

$$J_d = C_i \frac{dV_i}{dt} \tag{3.40}$$

where J_d = displacement current density

C_i = insulator capacitance per unit area

V_i = transient voltage across the capacitance

The generation current density can be written as

$$J_g = \frac{q}{2} \int_0^\infty \frac{dn}{dt}\, dx + \frac{q}{2} \int_0^\infty \frac{dp}{dt}\, dx \tag{3.41}$$

where $\frac{dn}{dt}$ and $\frac{dp}{dt}$ are the net rate of change of electrons and holes. Using the Shockley-Read-Hall theory [128] for a single trap level, $\frac{dn}{dt}$, $\frac{dp}{dt}$ are:

$$U_b = -\frac{dn}{dt} = -\frac{dp}{dt} = \frac{pn - n_i^2}{(n + n_1)\,\tau_{po} + (p + p_1)\,\tau_{no}} \tag{3.42}$$

where U_b = net rate of change of electrons or holes due to a bulk trap level

$n_1 = n_i e^{\frac{E_T - E_i}{K_B T}}$ = electron concentration if the Fermi level was at the bulk trap level,

$p_1 = n_i e^{\frac{-(E_T - E_i)}{K_B T}}$ = hole concentration if the Fermi level was at the bulk trap level,

n, p = total electron and hole concentrations.

$\tau_{po} = (C_p N_T)^{-1}$ = hole lifetime, N_T = bulk trap density (3.43a)

$\tau_{no} = (C_n N_T)^{-1}$ = electron lifetime (3.43b)

and C_p, C_n = hole and electron capture probability rates ($cm^3\ sec^{-1}$).

The equality of $\frac{dn}{dt}$ and $\frac{dp}{dt}$ is an approximation which is valid when the bulk trap occupancy is time independent (a reasonable assumption for g-r centers). The validity of this assumption should be checked especially in the initial phases of the transient response. In C-t measurements the depletion approximation is used during the transient ($np << n_i^2$) which simplifies (3.42) as follows

$$U_b = \frac{-n_i^2}{n_1 \tau_{po} + p_1 \tau_{no}} = \tau_{po} \exp\left[\frac{(E_T - E_i)}{K_B T}\right] + \tau_{no} \exp\left[\frac{-(E_T - E_i)}{K_B T}\right] \quad (3.44)$$

The generation lifetime (τ_g) is defined by the following equation:

$$U_b = -\frac{n_i}{\tau_g}$$

Thus: $$\tau_g = \tau_{po} \exp\left[\frac{(E_T - E_i)}{K_B T}\right] + \tau_{no} \exp\left[\frac{-(E_T - E_i)}{K_B T}\right] \quad (3.46)$$

In C-t measurements the assumpiton ($np << n_i^2$) is only valid in a portion of the transient response and using (3.44) out of this region results in erroneous estimation of τ_g [127]. The rate equation for TAV transient can be established by equating J_d and J_g from (3.40) and (3.41) and also using the following equation:

$$V_t = V_i + V_s \,, \quad (3.47a)$$

$$V_i = \frac{-Q_{sc}}{C_i} \quad (3.47b)$$

where Q_{sc} = change in the space charge density due to V_t

V_s = change in the surface potential due to V_t

V_t = TAV transient amplitude (figure 3.20).

Equation (3.47) can be considered as a small signal version of equations (3.5) or (3.28). For simplicity no other sign such as Δ is used. The depletion approximation cannot be used for the TAV measurements, due to the small amplitude of the TAV signal. The exact rate equation can be obtained by using equations (3.40)-(3.43), (3.47). In order to obtain U_b, the continuity and Poisson equations should be solved simultaneously with equation (3.42). These equations are repeated for completeness.

The continuity equations for electrons and holes are:

$$\frac{\partial n}{\partial t} = D_n \nabla^2 n + \mu n \nabla(nE) - U_b \quad (3.48a)$$

$$\frac{\partial p}{\partial t} = D_p \nabla^2 p - \mu p \nabla(pE) - U_b \quad (3.48b)$$

U_b is defined in equation (3.42),

$$E = -\nabla\phi,\ \nabla^2\phi = -\frac{\rho}{\varepsilon},\ \rho = q(p - n + N_D - N_A) \qquad (3.49)$$

It should be noted that in the continuity equations which were used to calculate the TAV amplitude in Chapter 2, U_b was neglected (equations (2.9), (2.10)). This is a reasonable assumption because these were the ac equations at SAW frequency and g-r centers do not respond at SAW frequency. The equations in this chapter are related to the TAV transients nd therefore they are time averaged with respect to the SAW frequency. By solving equations (3.40)-(3.49), using numerical techniques, the transient behavior of the TAV signal can be obtained and the dependency of the transient time constant on the carrier lifetime can be found.

An approximation to the above equations can be obtained by the following steps (figure 3.23). 1) The space charge region at any given bias voltage is replaced by a region with the same average carrier concentrations ($\bar{p}$, $\bar{n}$) but at the flat band condition. This step is discussed in detail in Section 3.3.1. 2) After the application of the rf pulse the charge polarization in the semiconductor takes place. The majority carrier concentration drops in a thickness on the order of a Debye length. Due to the nonequilibrium condition in this region ($np < n_i^2$) the generation process begins. It is assumed that as the minority carriers are being generated, the thickness of the generation volume decreases (W_t). 3) It is considered that the region ($\bar{L}_D - W_t$) has reached the equilibrium, and a constant average carrier

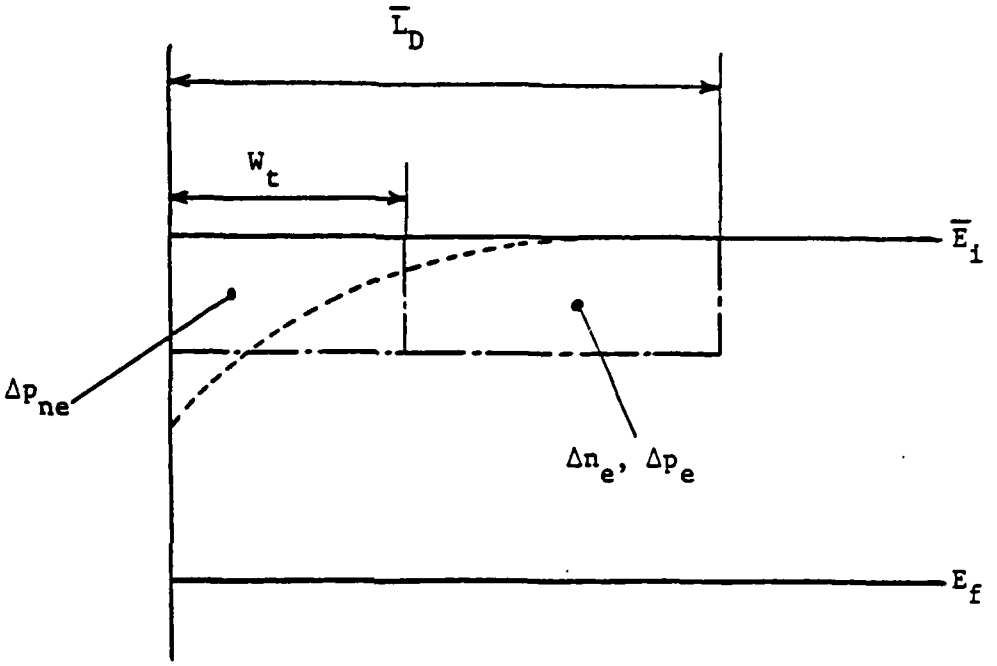


Figure 3.23 The approximate band diagram, used in formulating the TAV transient response.

concentration is assumed throughout this region. The equilibrium excess hole and electron concentrations in this region, are Δp_e, Δn_e. 4) In order to approximate U_b in equation (3.42) it is assumed that the majority carrier concentration is lowered with an average value Δp_{ne} which is constant within the nonequilibrium region (thickness = W_t). At steady state np becomes equal to n_i^2 in the whole interaction region and U_b, J_d, J_g (3.40)-(3.42) diminish. Using the above assumptions the following equations can be obtained

$$U_b \simeq \frac{-\bar{n}\,\Delta p_{ne}}{(\bar{n} + n_1)\,\tau_{po} + (\bar{p} - \Delta p_{ne} + p_1)\,\tau_{no}} = \frac{-\Delta p_{ne}}{\tau_{mg}} \qquad (3.51)$$

and

$$\tau_{mg} = \frac{(\bar{n} + n_1)\,\tau_{po} + (\bar{p} - \Delta p_{ne} + p_1)\,\tau_{no}}{\bar{n}} \qquad (3.52)$$

Equation (3.51) is valid within W_t region (figure 3.23).

Substituting (3.51) in (3.41) yields

$$J_g \simeq \frac{q\,W_t\,\Delta p_{ne}}{\tau_{mg}} \qquad (3.53)$$

Considering (3.40), (3.47b) the following equation is obtained:

$$J_d = \frac{-d\,Q_{sc}}{dt} \qquad (3.54)$$

and Q_{sc} is:

$$Q_{sc} = q[W_t\,\Delta p_{ne} + (\bar{L}_D - W_t)\,(\Delta n_e + \Delta p_e)] \qquad (3.55)$$

In equation (3.55) Δn_e and Δp_e can be approximated in the equilibrium region by:

$$\Delta n_e \simeq \bar{n}\,\bar{v}$$

$$\Delta p_e \simeq \bar{p}\,\bar{v}$$

where $\bar{v}$ is the average band bending in $\frac{K_B T}{q}$ units (it is assumed that the band bending is constant throughout this region). The above equations are valid if $\bar{v} < 1$. If the second term in the right hand side of the equation (3.55) can be neglected in the early stages of the transient response, then by equating (3.53) and (3.54), and substituting from (3.55), the approximate rate equation would be:

$$\frac{dW_t}{dt} = - \frac{W_t}{\tau_{mg}} \tag{3.56}$$

Thus the waveform will be an exponential with a time constant (τ_{eff}) which is equal to τ_{mg}. The validity of the above assumption can be checked by observing the form of the experimental TAV versus time curve. Different approximations of equation (3.55) can be considered which will result in different forms of the TAV transient responses. The proper approximation should be used by comparing its result to the experimental measurement. For the experiments reported in the next chapter, the TAV transient is exponential (similar to figure 3.4) and equation (3.56) can be considered. The assumption that the bulk trap occupancy is time independent, which is used in the above discussions might not be valid in some parts of the transient. In this case the rate equations for bulk trap occupancy (not the g-r centers) should also be included, and the time constants are strongly a function of the electron and hole emission rates.

The bulk trap levels below E_i (figure 3.22) dominate the bulk response in the range of the bias voltages discussed in this

section (midgap to weak inversion). The reason is that they exhibit cross over with the Fermi level. For these traps $p_1 >> n_1$. By using this assumption and equations (3.46), (3.52), (3.56) the following equation can be obtained:

$$\tau_{eff} \simeq \tau_{mg} \simeq \left(1 + \frac{\bar{p} - \Delta p_{ne}}{p_1}\right)\left(\frac{n_i}{\bar{n}}\right)\tau_g \qquad (3.57)$$

For bias voltages where $\bar{p}$ is less than an order of magnitude larger than n_i, (3.57) can be reduced to:

$$\tau_{eff} \simeq \left(\frac{n_i}{\bar{n}}\right)\tau_g \qquad (3.58)$$

For large values of $\bar{p}$ (3.57) can be written as:

$$\tau_{eff} \simeq \left(1 + \frac{\bar{p}}{p_1}\right)\left(\frac{n_i}{\bar{n}}\right)\tau_g \qquad (3.59)$$

Equations (3.57)-(3.59) are approximated and they can be used for an order of magnitude estimation of τ_g. It is shown that the measured lifetime (τ_{eff}) is a function of τ_g with an amplification factor. This factor is a function of $\bar{p}$, $\bar{n}$ at any bias voltage and also a function of p_1, n_1, which are characteristics of the trap levels. To extract the value of τ_g with a reasonable precision from the measured τ_{eff}, both TAV-V_B and τ_{eff}-V_B plots should be used simultaneously. The TAV-V_B plot can provide the information about the surface potential and thus $\bar{p}$, $\bar{n}$ at any bias voltage (discussed in section 3.3.1). Nevertheless the TAV transient time constant measurements can be used for comparison testing between the wafers with similar substrate parameters which have undergone

different fabrication processes. This mode of operation is easier and can be used as a nondestructive tool to evaluate the effects of different parameters on a processing step in order to establish the optimum alternative. It can also be used for screening the wafers which undergo a specific fabrication process in the production lines. In the next chapter the experimental results on the effect of laser induced damage gettering, etching and polishing are presented.

In the range of bias voltages where the surface g-r becomes more important (figure 3.21b) the measured τ_{eff} can be related to surface generation velocity (S_g) as follows:

$$\tau_{eff} \simeq \left(1 + \frac{p_s}{p_{ls}}\right)\left(\frac{n_i}{n_s}\right) \frac{\bar{L}_D}{S_g} \tag{3.60}$$

where p_s, n_s = electron and hole concentrations at the surface

$\bar{L}_D$ = average Debye length in the depleted region

$p_{ls} = n_i\, e^{\frac{(E_{it} - E_i)}{KT}}$, E_{it} = energy level of the interface trap.

In deriving equation (3.60) a similar procedure as for equation (3.57) is used, except now:

$$U_s = n_i\, S_g \tag{3.61}$$

where U_s = the net rate of change of the electron and hole concentrations at the surface (per unit area).

In the bias ranges where both bulk and surface effects are important, τ_{eff} can be written as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{mg}} + \frac{S_{mg}}{\bar{L}_D} \tag{3.62}$$

where τ_{mg} is defined in (3.57)-(3.59) and

$$S_{mg} = \frac{S_g}{\left(1 + \frac{p_s}{p_{1s}}\right)\left(\frac{n_i}{n_s}\right)} \tag{3.63}$$

At bias voltages where the surface is strongly inverted the TAV polarity changes to positive and the transient time constant is related to the recombination lifetime. The reason is that the non-linear interaction tends to decrease the minority carrier concentration in the inversion region. The effect of nonlinear interaction on the band bending and TAV polarity is shown in figure 3.24. Even though the interface traps are almost completely ineffective in this regime, this conditions is not used extensively because of the poorer signal to noise ratio.

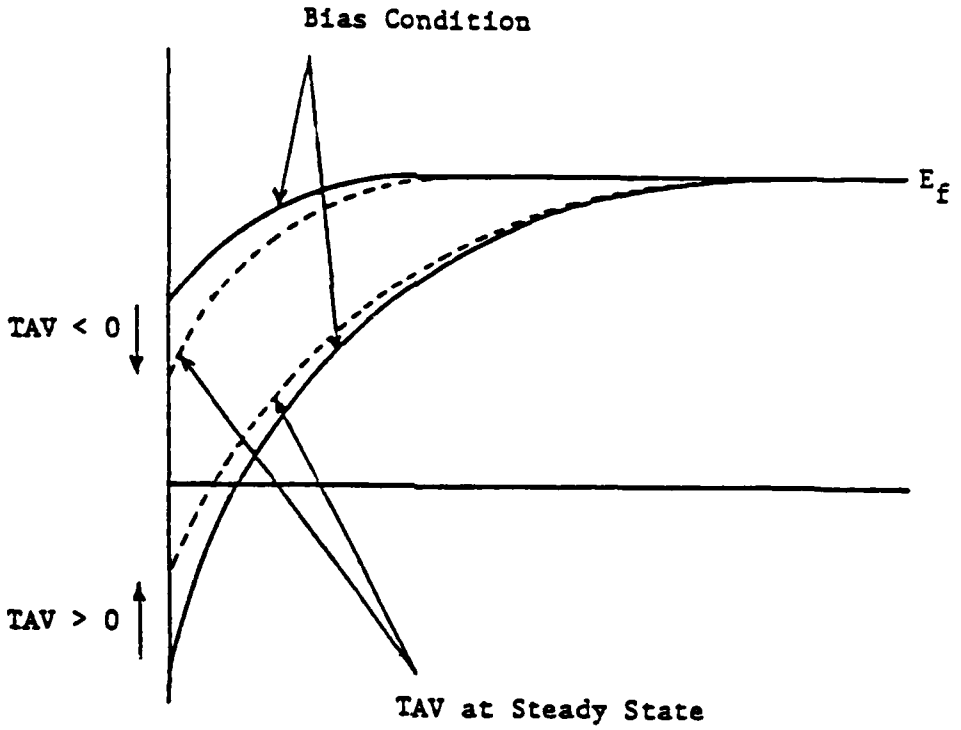


Figure 3.24 The effect of the TAV on the average surface potential under different biasing conditions (depletion and inversion). In all cases the TAV modulates the surface potential towards the midgap.

CHAPTER 4

EXPERIMENTAL RESULTS AND DISCUSSIONS OF THE TAV MEASUREMENTS: PROFILING AND TRANSIENT TIME CONSTANT METHODS

In Chapter 3, the theoretical foundations and the experimental apparatus for the TAV amplitude and time constant measurements under the application of the bias voltage are presented. A profiling procedure which is applicable to the TAV measurements is discussed. In this chapter the experimental results of the TAV measurements as applied to the device grade silicon wafers are presented. The following experiments are reported:

- Depth profiling of the majority carrier concentration for the phosphorous implanted high resistivity silicon substrates [51,52].
- Measurements of the TAV transient time constant in order to monitor the effects of the laser induced damaged (LID) gettering, etching and polishing on the silicon wafers [61,62].

The TAV experimental results which are used to obtain the interface charges and flatband voltage of the uniformly doped silicon samples have already been discussed in Chapter 3.

4.1 Depth Profiling

The delay line structure and experimental apparatus for the TAV amplitude versus bias voltage (TAV-V_B) measurements which are used for depth profiling is presented in Chapter 3 (figures

3.1-3.3). In the following experiments the rf pulse applied to the input transducer is at 110 MHz and its amplitude is about 10 volts p/p (50 Ω input resistance). The pulse width is about 1 msec with the repetition frequency of about 40 Hz. The TAV amplitude is measured by the lock in amplifier. The bias voltage is a slow varying ramp with the voltage scan rate on the order of 100 mV/sec.

The samples under test are a series of ion implanted silicon wafers. The substrate has the following paramaters: <100> surface, both faces polished, p type, high resistivity ($\rho \simeq 2800$ Ω cm, $N_A \simeq 5 \times 10^{12}$ cm^{-3}). Both faces are steam oxidized with the oxide thickness of about 200 A°. Phosphorous is implanted at 7° off axis through the oxide. Implants are activated by furnace heat treatment at $1000^{\circ}C$ for 60 minutes in nitrogen ambient. The implantation ion doses and energies are as follows

Sample #	Energy (KeV)	Dose (Ions/cm^2)
1	100	1×10^{11}
2	100	1×10^{12}
3	100	1×10^{13}
4	200	1×10^{11}
5	200	1×10^{12}
6	200	1×10^{13}
8	no implant	

The phosphorous depth profiles as calculated from the symmetric Gaussian distribution functions are shown in figure 4.1. The projected range (R_p), straggle (ΔR_p) and peak concentration are determined at different ion doses and energies [115]. The profiles can be calculated more accurately by using higher moment analysis [115,129,130]. In the three moment approach, two Gaussian curves with different straggles are joined at the projected range [129]. Four moment analysis includes the skewness and tailing properties of the profiles [130]. In the profiles shown in figure 4.1, the effect of dopant redistribution, caused by the diffusion during the annealing period is neglected.

The block diagram of the profiling procedure, using the TAV measurement is shown in figure 4.2. The following steps are taken:

1) The TAV-V_B curves are obtained as discussed in Chapter 3. The TAV-V_B plots for some of the ion implanted samples (#1,2,3,4) and the substrate (#8) are shown in figure 4.3 [51]. The substrate curve (similar to figure 3.16) shows a positive TAV at zero bias voltage, indicating a p type conductivity. By applying positive V_B the surface tends to accumulate and the TAV changes accordingly. The application of negative bias voltage changes the surface potential from depletion to inversion and the TAV polarity changes from negative to positive, indicating n type surface conductivity. The TAV plots for ion implanted samples exhibit a positive TAV at zero bias condition, indicating a compensated

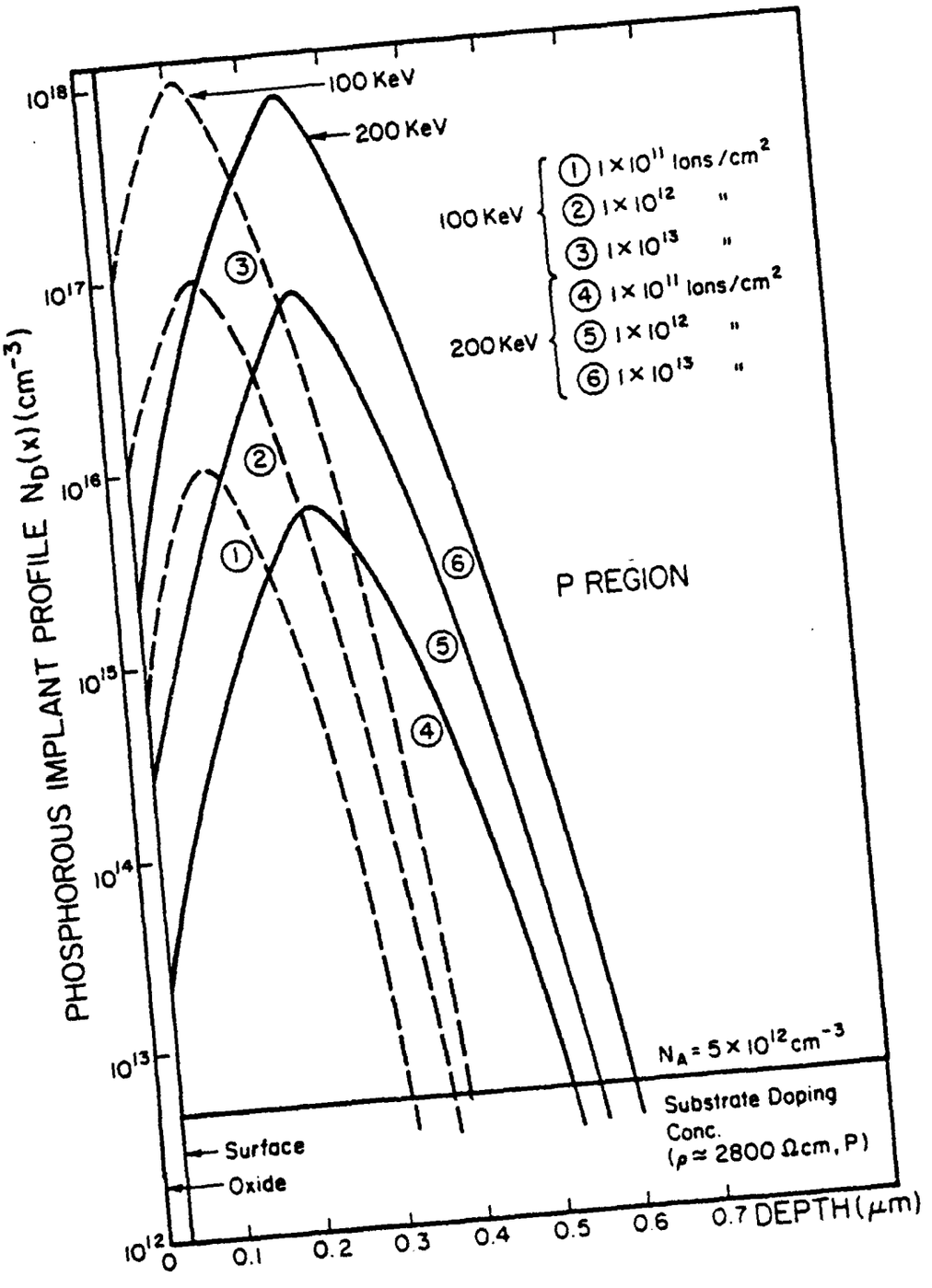


Figure 4.1 Calculated phosphorous implant profiles into high resistivity silicon substrate (P, ρ ≃ 2800 Ω cm).

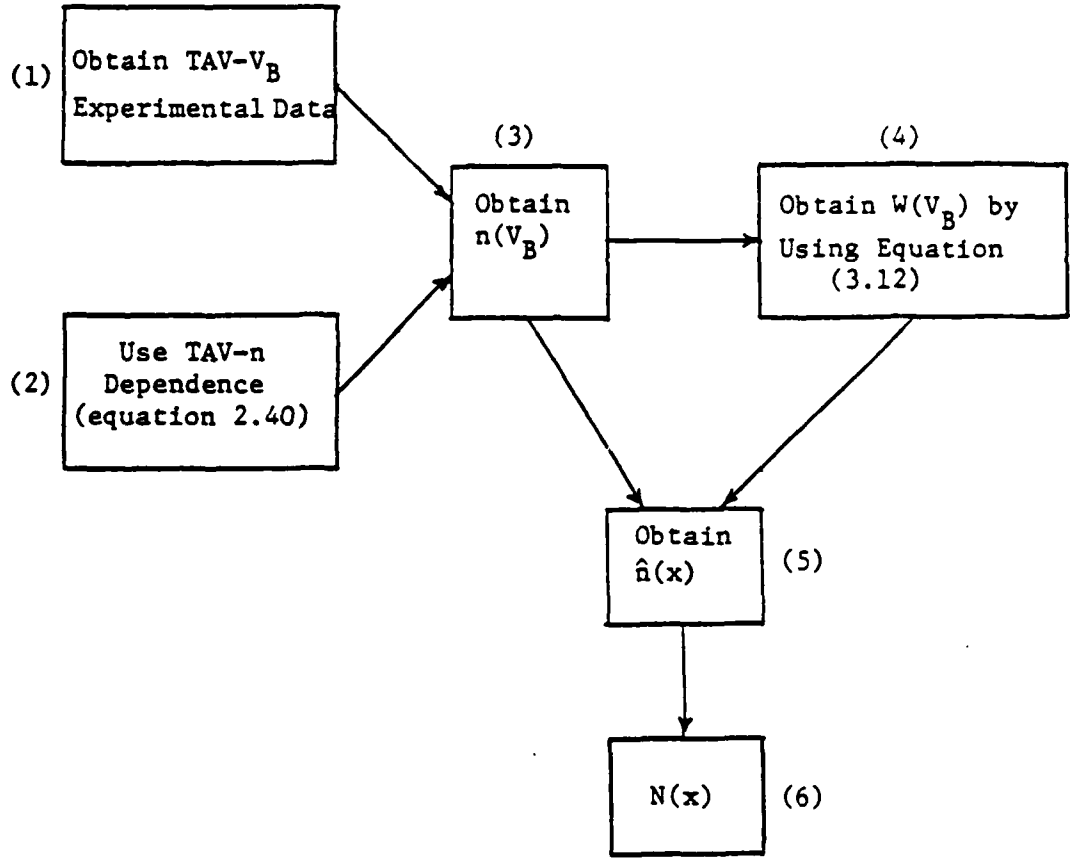


Figure 4.2 Block diagram of the profiling procedure, using TAV-V_B measurements.

surface (curve (2) is an anomaly and will be discussed later). By applying positive bias voltage, the ion implanted region (n type) becomes depleted and the TAV amplitude goes through the variations, reflecting the profile of the phosphorous implant. After a certain positive voltage the TAV polarity changes to negative, indicating the end of the implanted region or the onset of the surface inversion. Curve (2) in figure 4.3 shows an anomalous behavior. In this curve the TAV is positive at zero bias indicating a p type surface. One reason is attributed to the fact that the samples were sliced before the measurement and the leakage current at the edges might have affected the TAV-V_B curve. The other possibility is that the surface might indeed be p type at zero bias due to such effects as the nonuniform distribution of the p dopant in the substrate. More than an order of magnitude increase in the p dopant near the surface is observed for some of the substrates, using the spreading resistance measurements. Another effect to be considered is the depleting effect of the rf probing electric field. This effect can be eliminated by reducing the SAW power.

2,3) The relationship between the TAV amplitude and the carrier concentration as developed in Chapter 2 (equation (2.40)) is used to obtain the $n(V_B)$ curve. In doing so a calibration curve is needed to estimate the value of V_o in equation (2.40). TAV amplitude can be calibrated versus different samples with known resistivity for any experimental setup [42]. In the following experiments the reference is estimated by using the value of

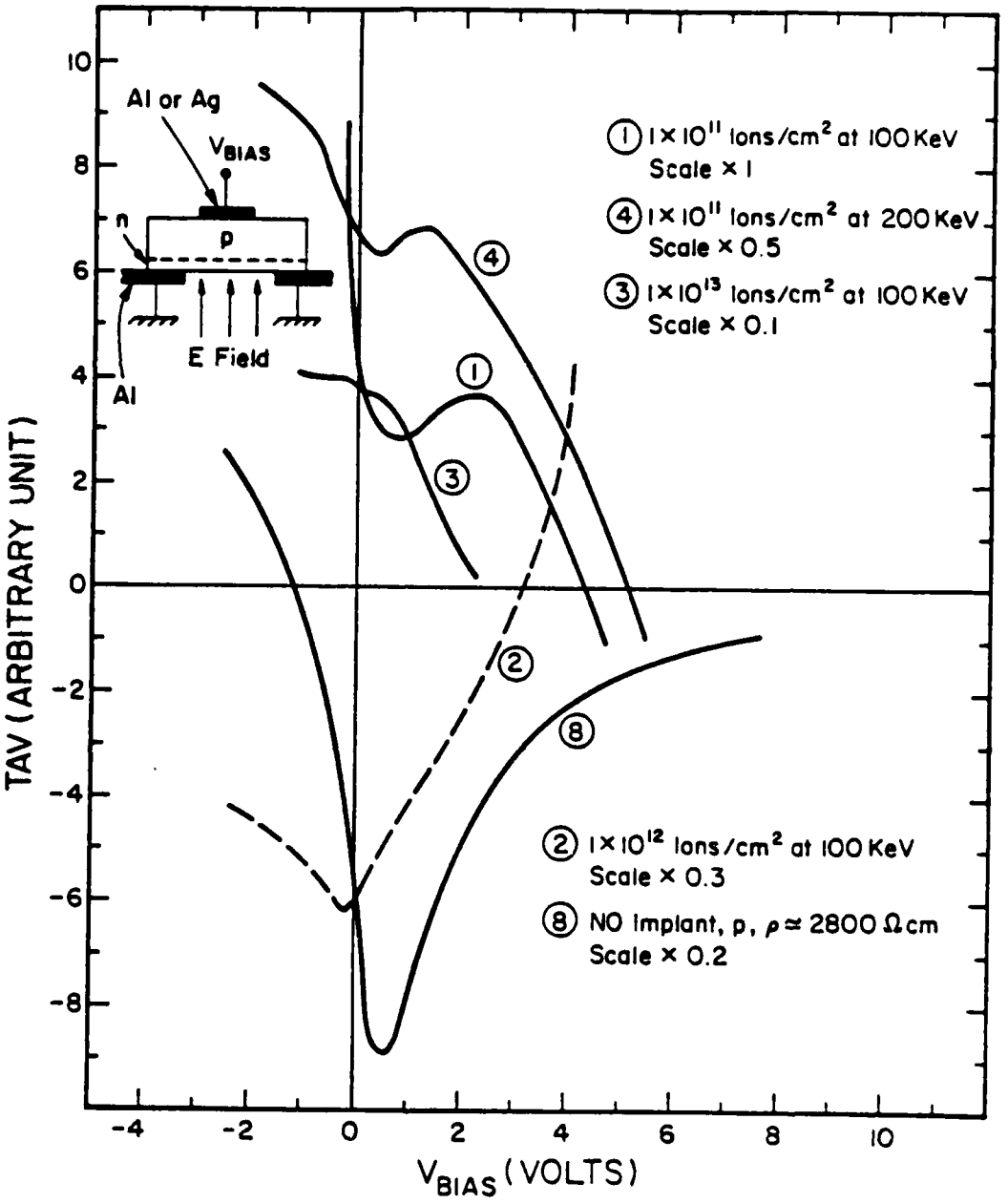


Figure 4.3 Experimental TAV-V_B plots for the ion-implanted samples and the high resistivity substrate.

the carrier concentration at the peak of the implant profile. For example, the relative minimum of the TAV-V_B curve for sample #1 (figure 4.3, $V_B \simeq 0.7$ volts) corresponds to the peak carrier concentration of the phosphorous profile for this sample. The reason is that for the above implanted samples, the majority carrier concentration is high enough that the negative slope side of the TAV-n curve (figure 2.3a) can be considered. A good estimation of V_o is obtained by using the peak concentration as measured by the spreading resistance technique.

4) In order to obtain the depth profiles, the information about the depletion width at each bias voltage is eeeded. The depletion width is calculated by using equation (3.12). Considering the $n(V_B)$ curve, the bias voltage in the depletion direction is divided into equal voltage increments ($\Delta V(m)$, figure 4.4). At each $\Delta V(m)$ an average value of majority carrier concentration is estimated ($n(m)$). Then equation (3.12) is used to calculate $W(m)$ at any bias voltage, leading to $W(V_B)$. In equation (3.12) the zero depletion width is corresponded to the flatband voltage (i.e., $W = 0$ at $V_B = V_{FB}$). For the n implanted samples in these experiments, the flatband voltage is assumed to be zero. The reason is that, since the oxide charge is invariably positive, it tends to modulate the surface potential of the n surface towards flatband and accumulation. In this regime the surface potential is not a strong function of V_B and the zero flatband approximation does not introduce an appreciable error. The validity of these

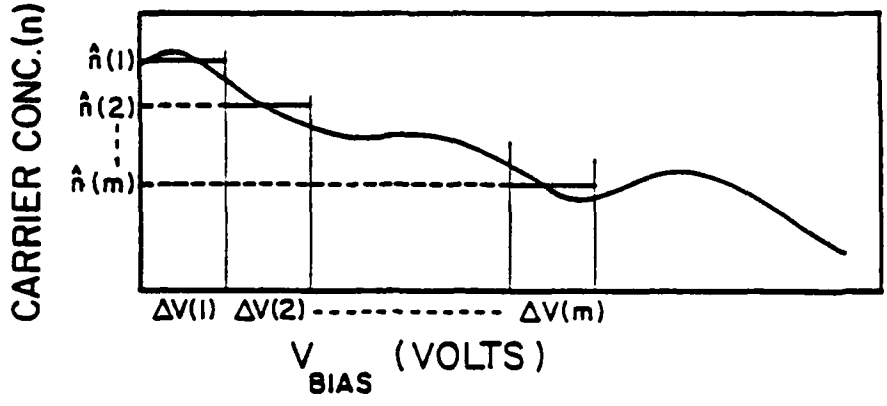


Figure 4.4 Average majority carrier concentration at corresponding voltage increment, used to calculate the depletion width as a function of the bias voltage (equation (3.12)).

assumptions are checked later by choosing different values of V_{FB} and comparing the calculated profile with the results obtained from the spreading resistance measurement. If the profile is p type near the surface, the oxide charge causes a depletion and the flatband voltage can be estimated by using the procedure which is discussed in the previous chapter and by iteration. A general procedure which provides the exact value of V_{FB} at any arbitrary doping profile does not seem to be feasible and utilizing the proper approximation for any specific case is more appropriate.

5) In steps 3, 4 the majority carrier concentration and the depletion width are obtained as a function of depleting bias voltage. By combining these results the average majority carrier concentration profile ($\hat{n}(x)$) can be obtained. Figure 4.5 shows the $\hat{n}(x)$ for sample #4 (1×10^{11} ions/cm^2, 200 keV, solid line) along with the implant profile obtained from the spreading resistance measurement (dotted line) [52]. The $\hat{n}(x)$ curve is obtained by assuming zero flatband voltage. In order to obtain N(x) from $\hat{n}(x)$, the corrections and approximations discussed in section 3.2.2, can be used. If the free carrier Debye averaging affect is neglected, then N(x) can be calculated from $\hat{n}(x)$ by using equation (3.18). Although the impurity concentration profile is sharper than the majority carrier profile at the high concentration gradient regions, the error does not exceed the data obtainable by the C-V techniques. The source of the error which is the spread of the majority carriers due to diffusion is inherent of the

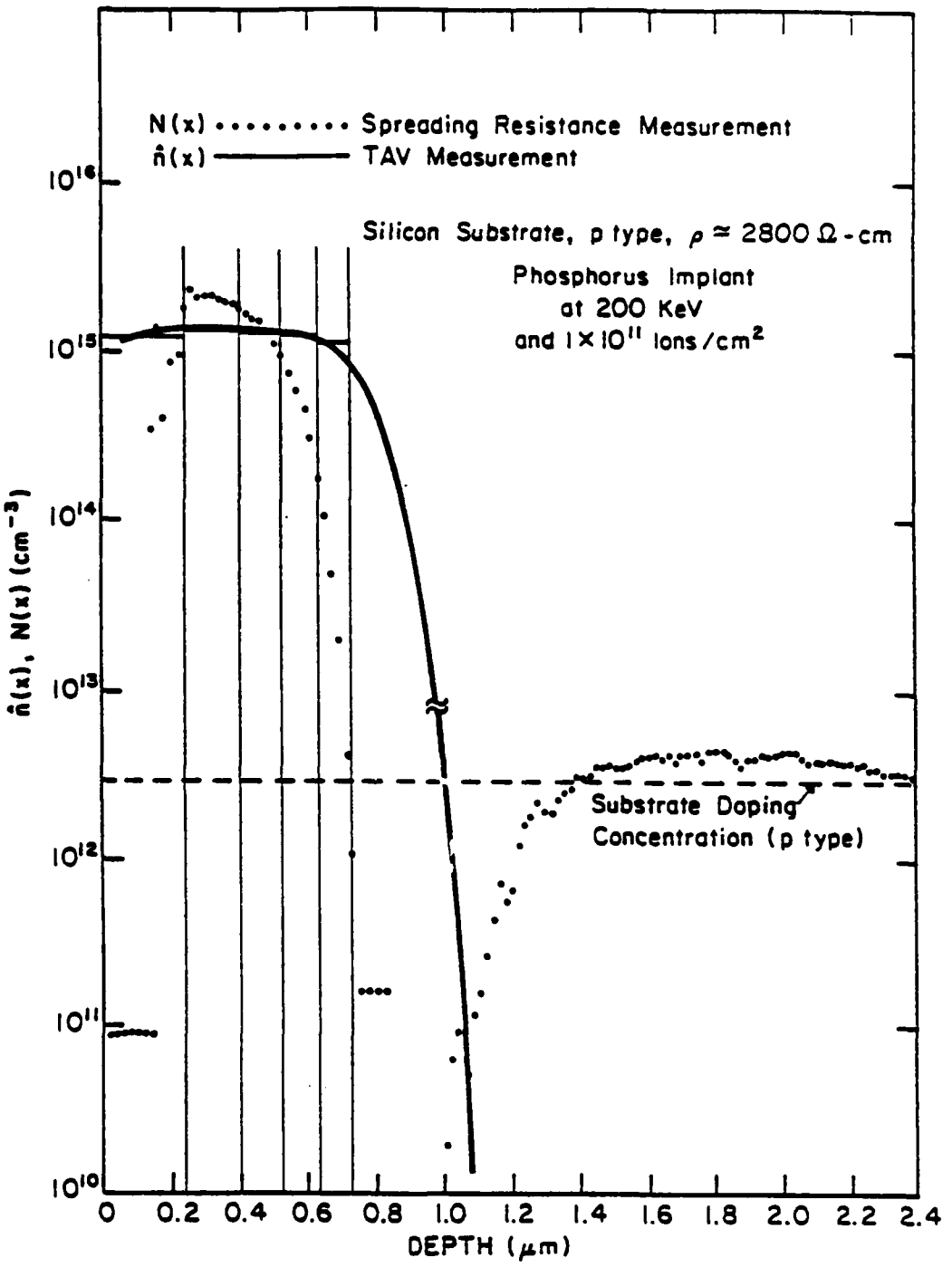


Figure 4.5 Average majority carrier and impurity density profiles of the phosphorous implanted high resistivity p type silicon substrate, as obtained by TAV and spreading resistance measurements.

measurements which monitor the carrier concentration without material removal. As discussed in Chapter 3, this error is more pronounced in the regions where the impurity concentration varies sharply in distances comparable to the Debye length. In the spreading resistance technique, the dopant density profile is obtained on a beveled sample, thus the carrier diffusion is eliminated. This technique is sensitive to the probe points condition and is subject to a large number of corrections. For more precise impurity profiling the material study methods, such as secondary ion mass spectroscopy (SIMS) and Rutherford back scattering (RBS) should be used. In any case, $\hat{n}(x)$ is measured by the TAV-V_B or C-V techniques provides a good estimation of the impurity doping profile in the distances larger than a few Debye length. The sensitivity of the TAV-V_B method is higher than C-V or SIMS techniques at low carrier concentrations and it is lower at high carrier concentrations. The measurable carrier concentration for silicon can be as low as 10^{12} cm^{-3} and the high limit is on the order of 10^{17} cm^{-3}.

The measured profiles are wider than the calculated profiles shown in figure 4.1. One reason is the nature of the phosphorous implant which exhibits a strong tailing in the deep region of the implant [131] due to channeling [132] or diffusion at implantation temperatures. The other reason is the redistribution of the impurity atoms under the annealing heat treatment, performed for impurity activation. The broken line at the end of

the $\hat{n}(x)$ curve in figure 4.5 corresponds to the TAV amplitude after the relative maximum in the TAV-V_B curve (figure 4.3). In this region the carrier concentration varies by several orders of magnitude and the TAV polarity changes from positive to negative. This polarity change can be due to the extension of the depletion region up to the p-n junction, resulting in the interaction of the probing electric field with the p type substrate. Therefore the termination of the n region is reflected in the TAV polarity change. The former phenomenon can be assumed to be dominant by considering the dopant profile in figure 4.5 (the depth of the implanted region is somehow smaller than the maximum depletion width). The surface inversion can be eliminated by using pulsed bias arrangement as discussed in section 3.2.2. It should be noted that the tested samples are inherently difficult to characterize because of the sharp changes in doping concentration in distances on the order of a Debye length. The profiles obtained for other implanted samples are similar to the presented profile with the shifted projected range along the depth axis and different peak concentrations which are dependent on the ion doses and energies.

4.2 TAV Transient Measurements on Silicon Wafers

In this section the experimental results of the TAV transient measurements (TAV-t) in monitoring the effects of LID gettering, etching and polishing on the imperfection density of silicon wafers are presented. The LID effectiveness is monitored by comparing the lifetimes and surface generation velocities in

two halves of the wafers, one of which has undergone the LID gettering at the back surface. The TAV-t results which are strongly affected by surface condition, indicate about twofold increase in the lifetime in the gettered area. The bulk generation lifetime measured by the capacitance-time (C-t) technique does not show this increase. The reason is attributed to the reduction of the surface generation velocity on the opposite side of the LID gettering area. To evaluate the effects of etching and polishing on silicon wafers prior to the device fabrication, the TAV-t measurements under bias voltage are performed. The results indicate about two order of magnitude increase in τ_{eff} after etching and polishing due to the surface damage removal. In the above TAV-t experiments both oxidized and unoxidized samples are investigated without the fabrication of MOS structures. The discussions of the above topics are presented in the following.

4.2.1 Evaluation of the Laser Induced Damage Gettering Effect Using Lifetime Measurements [61]

The processes which are used to reduce the density of crystal defects and harmful impurities in the device region of the wafer are generally referred to as gettering processes. One area of increasing importance is the gettering by introducing damage to the back surface of the silicon wafers prior to device fabrication. The back surface lattice damage attracts and binds the crystal defects and metallic contamination, thus increasing the yield on the opposite (device) side [111-112]. The

effectiveness of the gettering technique is evaluated by the dislocation density it produces and the thermal stability of the damage. Another factor is the level of contamination introduced by the damaging process itself. Techniques such as grinding and sand blasting introduce an undesirable level of contamination, and the damage is not stable through the thermal cycles of a typical fabrication process. Laser induced damage (LID) is a promising technique that provides a less contaminating process and more stable (or refreshable) gettering sites [111]. The techniques to evaluate the extent of the gettering effectiveness and its persistence through the thermal cycles are either material study which requires some sort of mechanical damage to the wafer (cleavage, etching, ion milling) or the study of the electrical properties at the device side of the wafer. The latter encompasses such measurements as the junction yield evaluation and MOS capacitance measurements. In this section the application of the TAV transient measurements (TAV-t) as a nondestructive technique is demonstrated.

The samples under test are 4", <100> surface, p type silicon wafers (ρ = 11-16 Ωcm) with an oxide (dry-wet-dry) of about 5500 A^{o}. The LID is introduced on half of each wafer prior to oxidation with the other half left ungettered as the control sample. The LID is produced by Nd:YAG laser with 1.06 μm wavelength. The laser is pulsed with 15 KHz repetition rate and the pulse energy is 10 Joules/cm^2 with $\simeq$ 200 nsec duration. The

laser beam is focussed to a 60 μm spot size and the spot overlap is 50%. The damage depth induced by the beam is approximately 5 μm. Laser beam is scanned over the lines separated by about 0.5 mm and the time needed to cover half of the wafer is 60 seconds. The samples then undergo simulated thermal cycles (7~8 cycles) of a typical N-MOS fabrication process in order to reveal the persistence of the gettering effect after actual processes. The two wafers under study (A and B) have essentially the same characteristics but obtained from different vendors. For C-t measurements 60 mils Aℓ dots are evaporated on the oxide as MOS gate and Aℓ ohmic contact is provided on the back side.

The TAV transient waveform and circuit requirements are discussed in section 3.4.1 (figures 3.4, 3.19, 3.20). The rf pulse parameters are the same as discussed in the previous section (4.1). The measured time constant of the TAV transient (τ_{eff}) is shown in Table 4.1. This time constant is related to τ_g and S_g through equations (3.62) and (3.57)-(3-63). In this section τ_{eff} is measured at zero bias voltage and the surface generation velocity dominates the transient response. This effect is realized by measuring the bulk generation lifetime, using the C-t technique. The values of measured lifetime by TAV-t technique are in the 50-100 μsec range, whereas the bulk lifetime measured by C-t are in the 400-600 μsec range. The reason is the effect of surface generation velocity which is present in the TAV measurement. In C-t measurement, in order to avoid the surface generation, the MOS

		N_A (cm^{-3})	τ_g (μsec)	τ_g ratio LID/No LID	τ_{eff} (μsec)	S(cm/sec)	S ratio LID/ No LID
Sample A	No LID	7.8×10^{14}	394	1.5	44	0.29	0.48
	LID	6.0×10^{14}	596		92	0.14	
Sample B	No LID	8.8×10^{14}	464	1.1	43	0.30	0.47
	LID	8.9×10^{14}	522		92	0.14	
		(C-V)	(C-t)		(TAV)		

Table 4.1

Comparison of the lifetime and surface generation velocities in the LID and no LID regions of the silicon wafers

gate is pulsed between +10 to +20 volts in the strong inversion region as shown in figure 4.6. This figure shows the C-t plots of two MOS structures in the LID and no LID halves of the sample B. In strong inversion the effect of S_g can be neglected because the interface g-r centers are filled with electrons as discussed in section 3.4.2. The effect of S_g at the depleted (not inverted) periphery of the MOS gate can be easily neglected due to large gate diameter ($\simeq$ 1500 m) as compared to generation distance ($\simeq 4\ \tau_g\ S_g$ < 8 μm) [69,126]. The bulk lifetime (τ_g) is calculated from the C-t transient according to [68]. The results are shown in Table 4.1. In order to calculate τ_g, the value of N_A is needed which is obtained from the C-V measurement. Table 4.1 shows that τ_g is about a factor of eight times τ_{eff} which indicates the dominance of S_g in determining τ_{eff} (the surface is not inverted in measuring τ_{eff}). Thus by using equation (3.62) at near midgap condition, S_g can be estimated from τ_{eff} ($S_g \simeq \frac{L_D}{\tau_{eff}}$). The estimated values of S_g for LID and no LID regions of samples A and B are shown in Table 4.1. The Zerbst plots [67] are also used to verify the correct range of the surface generation velocity. To obtain the Zerbst plot the MOS gate is pulsed from accumulation (V_g = -20 volts) to strong inversion (V_g = +20 volts) as shown in figure 4.7. The Zerbst plot is then obtained as shown in figure 4.8. The value of the surface generation velocity can be estimated from the intercept of the extension of the linear region of the Zerbst plot with the vertical axis. This is an approximate value [127,128] and is

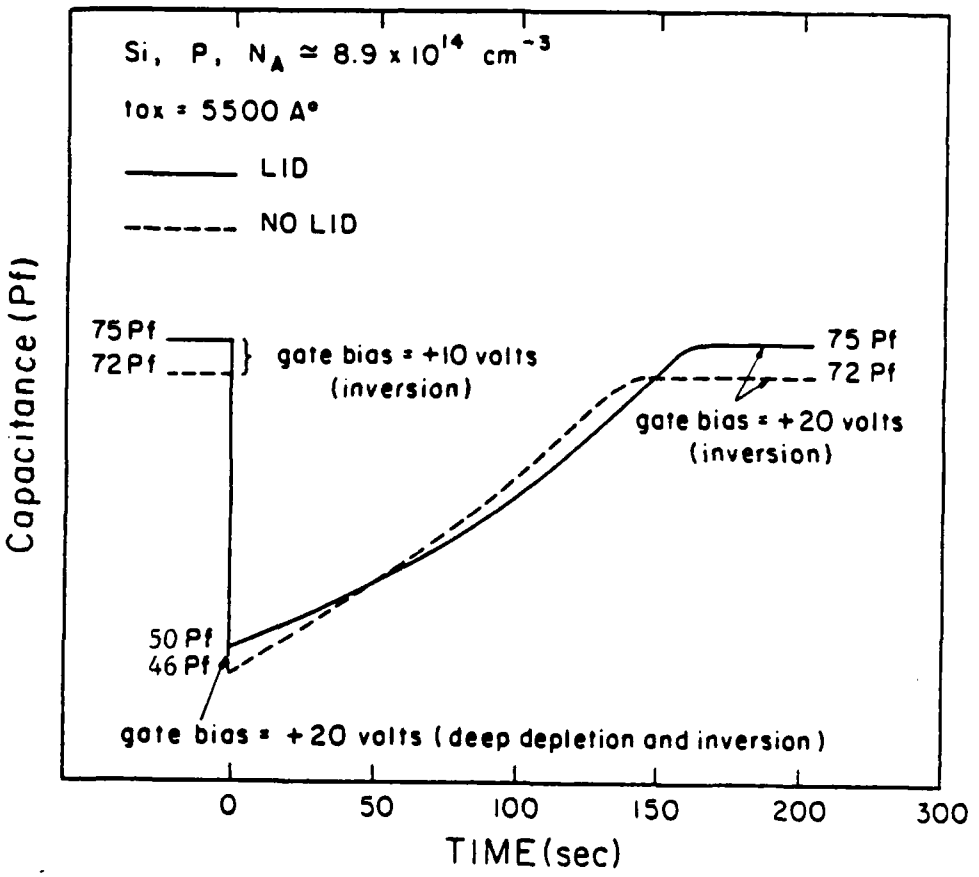


Figure 4.6 Capacitance time curves of the Si MOS structure for LID and No LID wafer halves. The gate bias is pulsed in the strong inversion condition to suppress the surface effects.

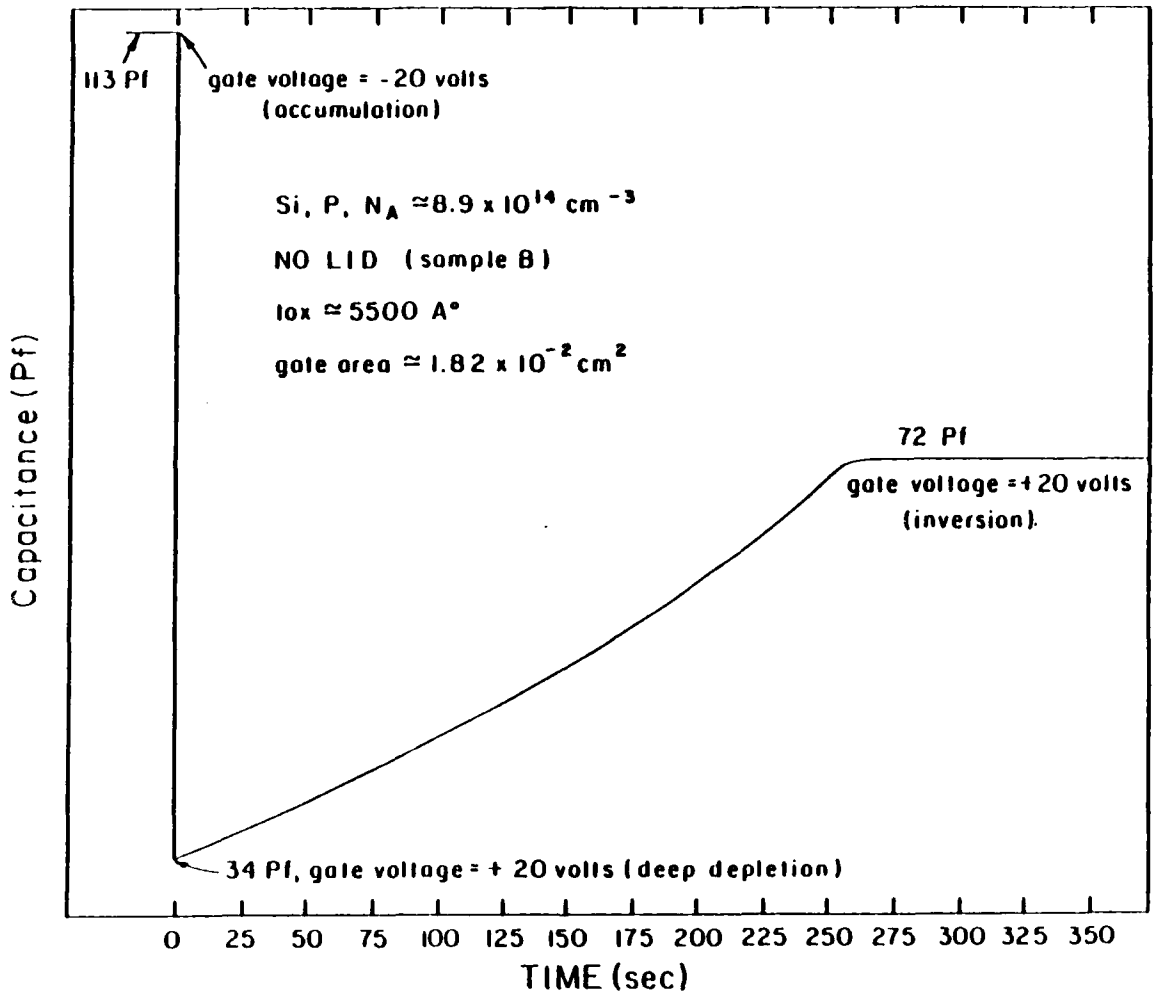


Figure 4.7 Capacitance time plot of the Si MOS structure. The gate bias is pulsed from the strong accumulation to the strong inversion in order to obtain the surface generation velocity and the generation lifetime by Zerbst method.

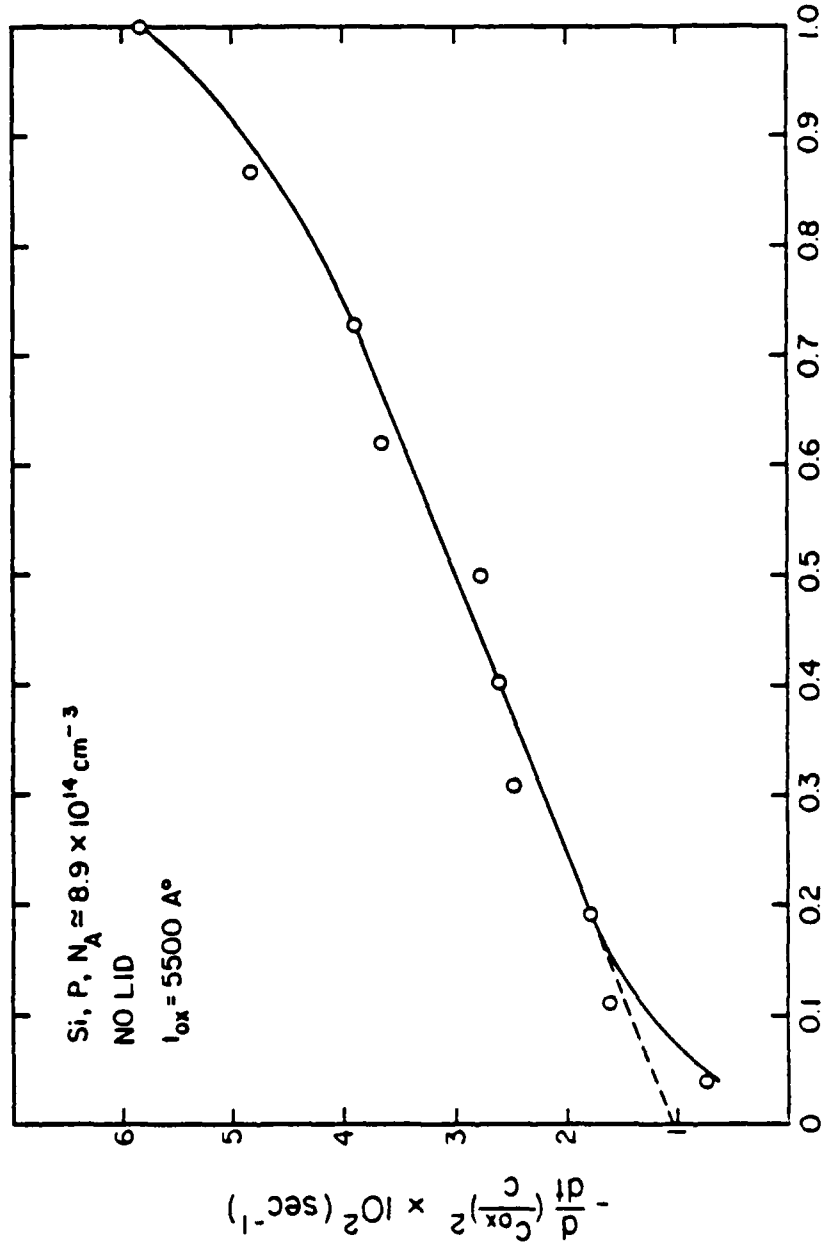


Figure 4.8 The Zerbst plot of the figure 4.7 C-t curve.

lower than the depleted surface generation velocity (S_g) due to the shielding of the surface states by the minority carriers, which takes place in a short time compared to the Zerbst transient time. The value of S_g from the Zerbst plot is about 0.1 cm/sec. which is in the same range, but lower than 0.3 cm/sec. which is obtained from the TAV measurement (Table 4.1, sample B, No LID).

Table 4.1 shows that the gettering effect is more pronounced in reducing the surface generation velocity rather than increasing the bulk lifetime. S_g is reduced by about a factor of 2 which indicates the reduction of the interface states and surface defect density by LID process, whereas the bulk generation lifetime is not appreciably affected by LID gettering. One reason might be due to the release of the point defects and contaminants from the gettered area due to the annealing of the dislocations and microcracks which are produced by LID. Therefore, after the simulated heat treatments, the bulk imperfection density for both LID and no LID halves are about the same. The released defects and impurities might not have had enough time to reach the surface, and therefore the surface generation velocity is lower for LID halves. Another reason can be the high quality of the starting material (long τ_g) which exhibits a low defect density in the bulk, such that the effect of LID is not appreciable. In these measurements the TAV-t is obtained by using C-t and TAV-t techniques. In the next section, the TAV-t measurements under applied bias voltage are performed and the effects of S_g and τ_g on the TAV transient response are discussed.

4.2.2 Evaluation of the Effects of Etching, Polishing and Forming Gas Annealing on Silicon Wafer Surface Properties [62]

In this section, 5" silicon wafers which have undergone different etching and polishing removal steps are studied, using TAV-t measurements. After the silicon wafers are sliced from the ingot by inner diameter slicing and edge rounded, they undergo etching and polishing prior to the device fabrication [133]. The chemical etching step is used to remove the damage and contamination which is left from the slicing process. The chemical etch removal is typically about one mil per side. After etching, the polishing step is performed to obtain the necessary flatness, specular surface, lack of features, and parallel surfaces of the wafer. In addition, polishing should not introduce any damage or contamination to the surface. Typical polish removal is on the order of a fraction of a mil. The extensive use of chemical etching followed by polishing is due to the fast removal rate by etching (economical, high throughput) and the required optical properties which can only be obtained by polishing (slow process). The extent of the damage removal by the above steps is monitored and compared by measuring the TAV transient time constant (τ_{eff}) which is related to τ_g and S_g as described in sections 3.4.2 and 3.4.3. τ_{eff} is also used to investigate the effect of forming gas annealing on the reduction of the interface states density for 3" oxidized silicon wafers.

To evaluate the damage removal properties of etching and polishing, a number of 5" silicon wafers are prepared. All the

wafers are sliced from CZ grown, p type, ρ = 11-16 Ωcm ingots, <100> surface and have undergone different etching and polishing times. Acid etching is used and the etchant mixture is 5:2:1 volume ratio of $HNO_3/HF/HC_2H_3O_2$. Etching is at room temperature and the etching barrel and wafer holder rotate during the process. For polishing, SiO_2 based slurries are used in the simultaneous two sided polishing arrangement. The amount of silicon removal for the wafers reported in this work (measured by capacitive probing) are as follows:

Wafer #	Chem. Etch Removal Both Sides (mils)	Polish Removal Both Sides (mils)	Total Removal Both Sides (mils)
14	0	0	0
13	0.4	0	0.4
16	7.1	0	7.1
10	0.4	2.2	2.6

Prior to the measurements, the wafers are cleaned in 8 steps, starting with the sulfuric/nitric acid organic material remover followed by immersion in acidic and basic hydrogen peroxide solutions in order to remove metallic contamination and ionic charges. To investigate the effect of forming gas annealing, five 3" silicon wafers are oxidized, annealed, cleaved and then random halves are annealed again in forming gas. The oxidation is dry-wet-dry and the oxide thickness is about 5500 A^o. Post oxidation annealing is performed in N_2 at 1000^{o}C. Forming gas (F.G.) annealing is in

5-10% H_2 in N_2 ambient, at 400°C for about 20 minutes.

The experimental apparatus for the TAV-t measurement is as discussed in section 3.4.1. In these measurements a special arrangement with a long delay line is used in order to accomodate 5" silicon wafers without slicing them. The rf frequency is 55 MHz and the pulse width is about 2 msec with the repetition frequency of about 15 Hz. The effects of τ_g and S_g in determining τ_{eff} can be approximately separated by the application of a depleting bias voltage as discussed in section 3.4.2. At surface potentials between flatband to near midgap the interface effects are dominant. By varying the surface potential towards midgap and weak inversion, the effect of surface g-r process goes through a peak and then reduces. At the bias voltages just before the polarity change of the TAV signal, it is assumed that τ_{eff} is dominantly determined by τ_g. These effects will be experimentally demonstrated. If a dc bias voltage (slow varying ramp) is used, the maximum depletion width, W_m, is less than 1 μm. Pulsed bias voltage can be used for the following conditions: 1) if the bulk g-r centers, deeper than W_m, are monitored, 2) to reduce the surface effects to a greater extent if the silicon surface exhibits a large interface state density. In this case the timing of the TAV measurement should be adjusted with respect to the bias pulse. The rf pulse should be delayed by about a fraction of a second (during this time the surface g-r centers become partially inactive) and the TAV-t measurement should be finished long before the inversion

layer sets in (the deep depletion regime). This timing arrangement is not difficult to attain, due to the long minority carrier response time in silicon (on the order of 10 seconds) and relatively short TAV-t time constant (on the order of msec).

The experimental results for differently etched and polished wafers are presented in figure 4.9. The τ_{eff} (at zero bias) is plotted as a function of position for different wafers. The value of τ_{eff} is related to τ_g and S_g through equations (3.57)-(3.63). The carrier lifetimes are on the order of 10 to 100 times smaller than τ_{eff} (due to the amplification factors, relating the τ_{eff} to the carrier lifetime, equations (3.57)-(3.59)) as will be shown later. The τ_{eff} plots in figure 4.9 are used for comparison of the defect density between the wafers with similar substrates which have undergone different etching and polishing steps. The plots indicate a large spatial variation of τ_{eff} for each wafer with generally lower values towards the edges. It is shown in figure 4.9 that by chemical etching and polishing, the lifetime increases which is an indication of the surface damage removal. Sample #16 (7.1 mils etching removal) exhibits about 10^2 times increases in the lifetime as compared to as sliced sample (#14). The wafer which is both etched and polished (#10) exhibits a longer average lifetime than the wafer which is only etched (#16) even though the total silicon removal is less. This result might indicate that polishing is to some extent, more effective than chemical etching in producing a damage free surface. The

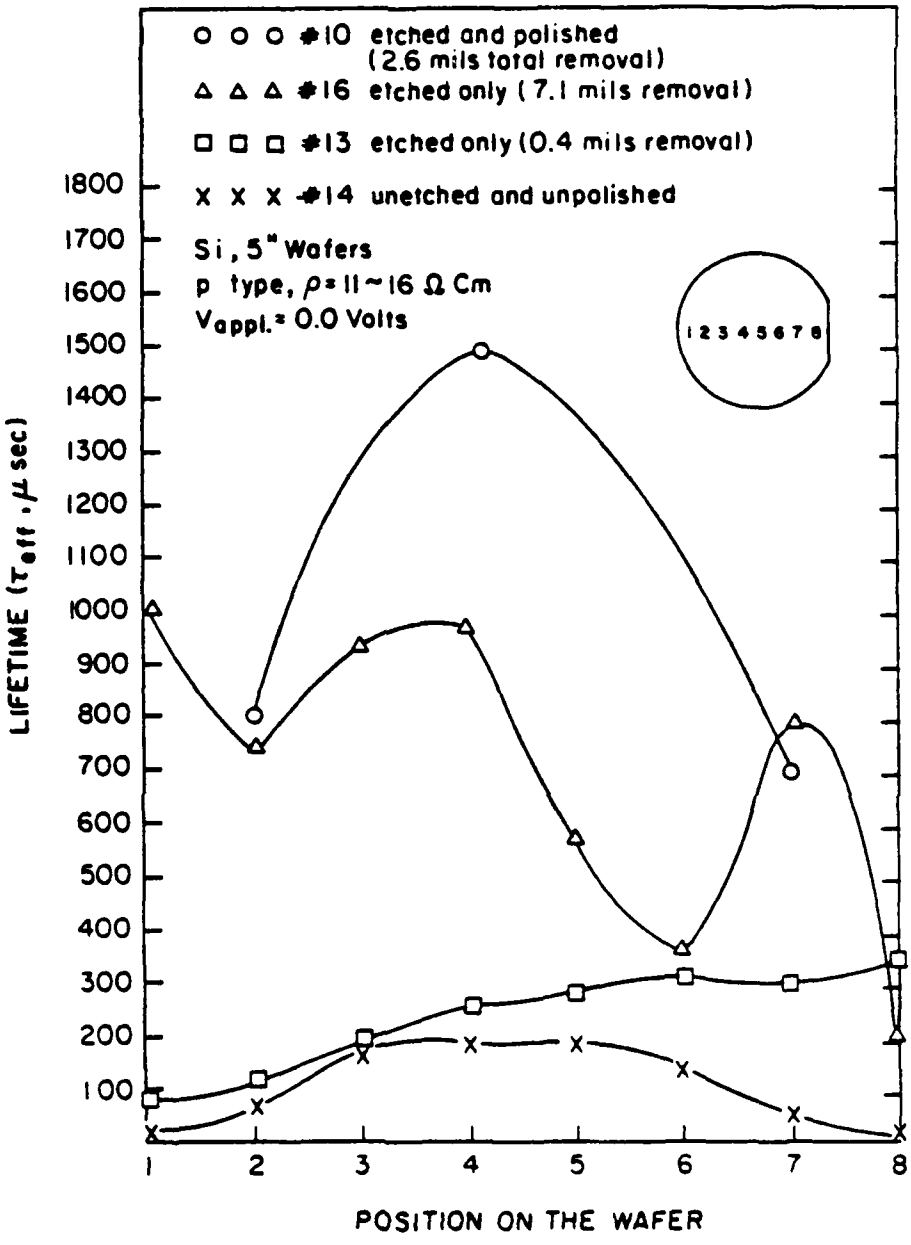


Figure 4.9 Spatial variations of the τ_{eff} for silicon wafers which have undergone different chemical etching and polishing steps.

argument is not conclusive and more experimental data is needed. One reason (in addition to the experimental error) is that #10 and #16 wafers were not specifically chosen as successive slices of an ingot. It is experimentally verified that the average values of τ_{eff} can vary by a factor of two for the samples which are sliced from different sections of an ingot, even if the wafers undergo the same etching and polishing steps [62].

In order to separate the contributions of τ_g and S_g to the measured τ_{eff}, the measurements under depleting bias voltage are performed. The results for as sliced sample (#14) are shown in figure 4.10 in the form of spatial variations of τ_{eff}, τ_{mg}, and S_{mg}. τ_{mg} and S_{mg} are approximately related to τ_g and S_g by equations (3.57) and (3.63). The depleting bias voltage is chosen at a value corresponding to the maximum measurable lifetime before the inversion. The reason is to quench the surface effect as much as possible by going further into the bulk (section 3.4). The measured lifetime under this bias voltage is approximately τ_{mg}, and S_{mg} is found from τ_{eff} and τ_{mg} at zero bias voltage (equation (3.63)). The variations of τ_{mg} and S_{mg} indicate that the increase of the surface gneeration velocity towards the wafer edges is dominantly responsible for the lower τ_{eff} close to the wafer periphery and the bulk generation lifetime varies only slightly across the wafer. This can be due to the handling damage around the wafer edges. The values of τ_g are about 10 to 100 times smaller than τ_{mg} and S_g is about 10 to 100 times larger than S_{mg}.

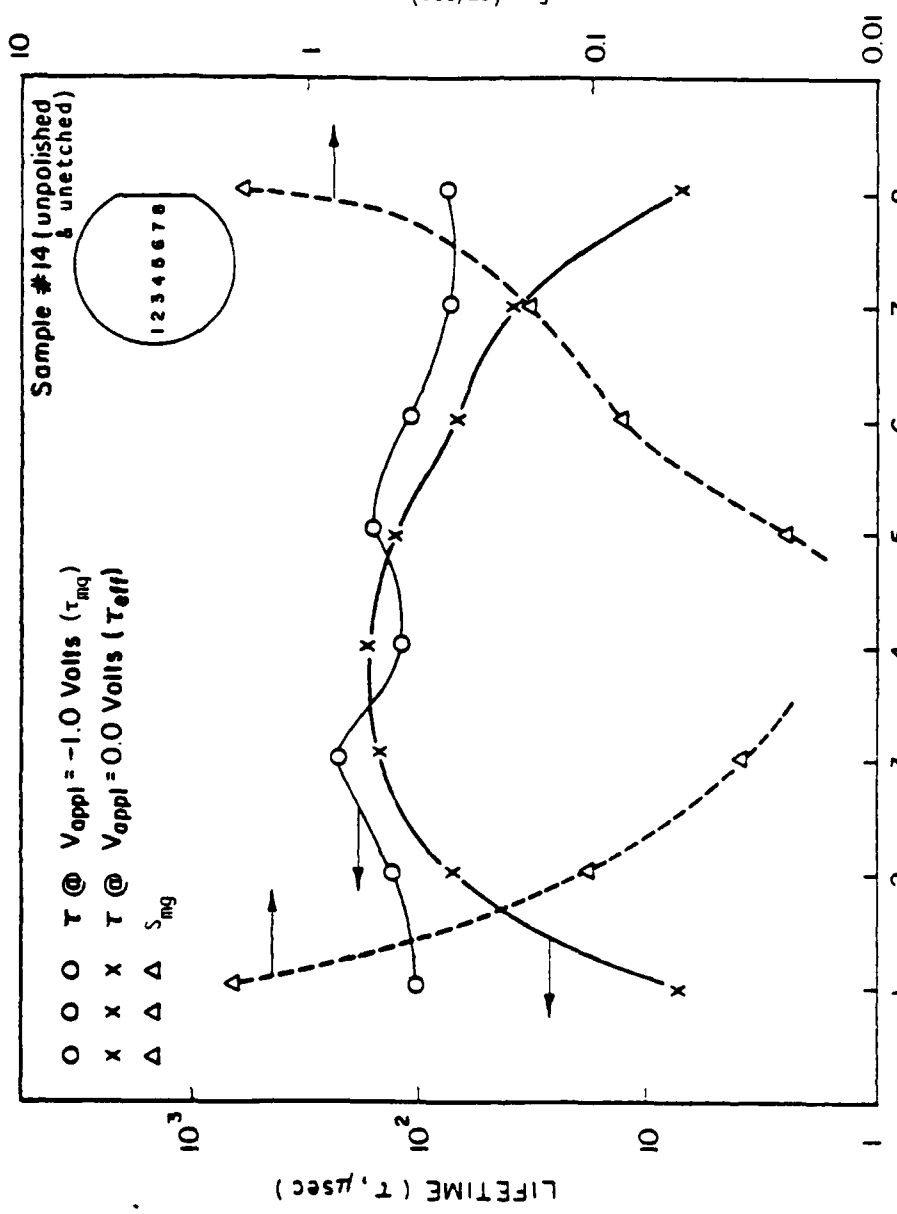


Figure 4.10 Spatial variations of τ_{eff}, τ_{mg} and S_{mg} for the as sliced silicon wafer (p type, ρ = 11-16 Ωcm).

The TAV amplitude and τ_{eff} dependence on the applied bias voltage (TAV-V_B and τ-V_B) for wafer #16 are shown in figure 4.11. The shapes of the plots are more or less the same for other samples with the major difference only in the TAV and τ absolute values. From the TAV-V_B curve, the value of surface potential (V_s) at each bias voltage can be estimated as discussed in section 3.3. The estimate of V_s is obtained by comparing the normalized TAV amplitude to the TAV-V_B curve, shown in figure 3.11. Therefore the values of $\bar{p}$, $\bar{n}$ can be obtained at each bias voltage (figure 3.10) and the amplification factor can be calculated (equations (3.57)-(3.63)). Different regions of the τ-V_B curve can be considered as follows. For V_B values varying from +2 volts to near zero, the surface potential changes from flatband towards depletion. In this region the response is governed by the majority carriers and the surface traps which only communicate with the majority carrier band (section 3.4.2, part A). The measured lifetime increases as the majority carrier concentration decreases at the surface, thus reducing the traps capture and emission rates. The τ-V_B curve goes through a peak (point B) and then drops to a minimum (point A) as the high density interface trap level (this time the g-r center) passes through the Fermi level (section 3.4.2, part B). From the τ-V_B structure in this region the energy position of the high density trap level can be estimated. By changing the bias voltage from zero to negative values the surface becomes more depleted and the effect of minority carriers increases.

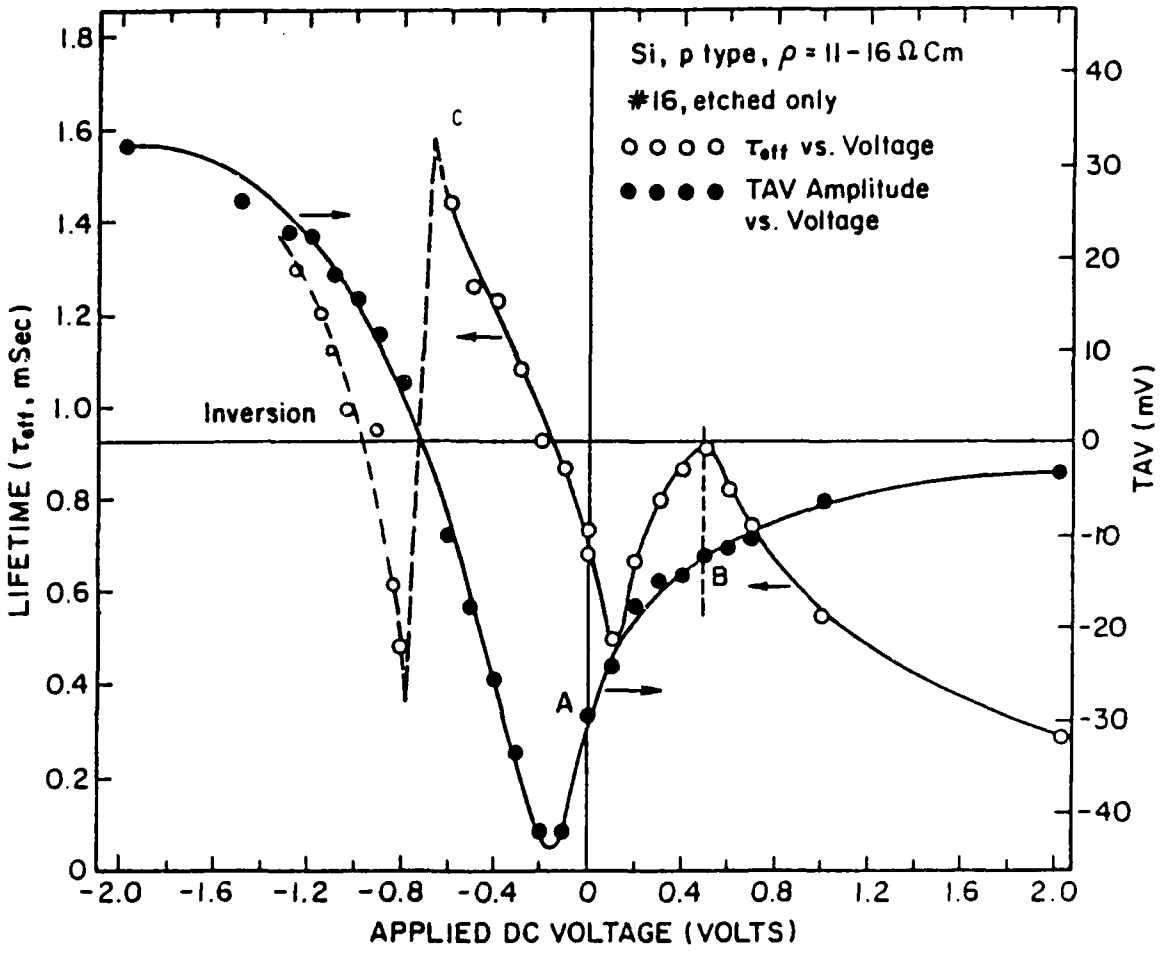


Figure 4.11 TAV amplitude and τ_{eff} dependence on the applied bias voltage for the etched silicon wafer.

In this bias range the high density interface trap level (at energy E_T which is below E_i as shown in figure 3.22) goes below E_f and the effectiveness of the interface g-r process is reduced (section 3.4.2, part C). Therefore the τ_{eff} increases until it reaches its maximum value (point C). At this value it is assumed that the surface g-r process can be neglected and τ_{eff} is only determined by τ_g as shown in equation (3.57). At bias voltages more negative than -0.8 volts, the surface is inverted and the τ_{eff} is related to the recombination lifetime (τ_{re}). It is shown that if the energy of the g-r center is not equal to E_i, then τ_{re} is smaller than τ_g [70]. This effect is observed in the τ-V_B curve in the inverted region. By considering the τ-V_B and TAV-V_B curves simultaneously, the energy of the trap level can be estimated at about 0.15 eV below E_i. The value of τ_g can then be extracted from the maximum value of τ_{eff} before the inversion (point C, figure 4.11) by using equation (3.59). The values of $\bar{p}$, $\bar{n}$ in this equation are obtained by using the TAV-V_B curve and estimating V_s as mentioned earlier. The amplification factor is about 20 at this point. Therefore the value of τ_g is approximately 700 μsec for this sample.

The effect of forming gas annealing on the τ_{eff} is demonstrated in Table 4.2. This table shows an average increase of the τ_{eff} on the order of 200 times for the forming gas annealed half wafers. This increase is partly due to the reduction of the interface states density and partly due to the change of the flatband voltage.

	τ_{eff} (μsec) @ zero bias voltage				
Sample #	1	2	3	4	5
No F.G.	2	100	1	1	1
F.G.	620	1600	120	500	220

Table 4.2

Comparison Between No F.G. and F.G. Annealed Half Wafers

CHAPTER 5

INVESTIGATION OF GaAs SURFACE AND GaAs/ANODIC OXIDE INTERFACE

In the past ten years there has been an increasing interest in the GaAs digital integrated circuit technology as well as in the more traditional microwave discrete devices. The advantages of GaAs over Si are the material properties, such as higher low field electron mobility which is an order of magnitude higher than Si and larger bandgap. Another advantage is the availability of GaAs as a good semi-insulating substrate. This property allows the self-isolation of the active devices either by mesa etching [134] or by simply using a planar double implanted approach [135]. Therefore the packing density for large scale integration (LSI) can be increased appreciably. Progress in GaAs LSI integrated circuits are mainly due to the technological advancements in fabrication processes and the availability of high quality semi-insulating GaAs substrate. 3", undoped, semi-insulating GaAs substrate grown by liquid encapsulated Czochralski method are available at the present time. In the processing areas such as the formation of a well controlled active layer (either by epitaxy or ion implantation) and fine line pattern replication there have been rapid improvements in the past few years. Although the GaAs technology is still far behind Si, in some areas such as very high speed integrated circuits (in the gigabit range) and microwave applications, the GaAs device performance cannot be matched by Si devices.

There are two basic approaches to GaAs FET, LSI circuits, one is the junction gate devices such as metal semiconductor field effect transistor (MESFET) and the other is insulated gate FET's (IGFET). The former technology is more rapidly advancing and is dominantly applied today for the fabrication of high speed logic circuits [135-137], even though the IGFET's have inherent device characteristic advantages. The reason is the difficulty encountered in the formation of a viable dielectric on the GaAs surface with acceptable interface states density. The inherent advantages of IGFET's over MESFET's are basically as follows. 1) The enhancement-mode MESFET's (E-MESFET's, normally off) are highly prefered in LSI circuits as compared to depletion mode MESFET's (D-MESFET's, normally on) due to the lower power consumption and less complex circuitry. The depletion mode MESFET's require dual power supply operation and level shifters in their circuit arrangement. But in the enhancement-mode the magnitude of the gate voltage swing is limited by the built-in potential of the gate junction. For inputs larger than the Schottky barrier built in potential (in the range of 0.5 volts), the channel current cannot be controlled and excessive gate current will be drawn. This limitation can cause an increase in the propagation delay and also is not desirable in microwave power devices. Another serious problem of the small logic swing is the need for a precise control of the pinch off voltage. In order to provide an adequate margin for LSI circuits, the logic swing should be at least an order of magnitude larger than the standard deviation of the pinch

off voltage. This effect dictates that the pinch off voltage should be controlled within tens of millivolts. Therefore the processing complexity increases dramatically as compared to D-MESFET technology. At the present time only D-MESFET's are fabricated at the LSI level. By using IGFET devices these limitations are eliminated.
2) The cutoff frequency of IGFET's is higher than MESFET's because of the higher decrease in the gate capacitance as compared to the decrease in the transconductance [108,110]. 3) The IGFET's exhibit lower input leakage current and simpler circuit configuration. The planar integrated circuit technology is used to fabricate an enhancement/depletion type MOSFET logic with a propagation delay of 72 ps and a power delay product of 139 fj for the 1.2 μm gate length [109]. The device can also be operated at a minimum power-delay product of 36 fj with a propagation delay of 157 ps.

The main problem of the devices made with the GaAs MIS technology is the anomalous behavior under dc and low frequency operation and the long term stability of the device. This behavior is believed to be due to the high density of trap levels present at the GaAs/insulator interface. The MIS structures made by low temperature oxidation of GaAs (wet anodic oxidation or plasma oxidation) exhibit superior interface characteristics as compared to other insulator structures [110]. The reason is generally due to the high temperature step involved in the deposition of the heteromorphic dielectrics and also GaAs thermal oxidation. The high temperature step is not desirable due to the high volatility of As and As oxides.

Therefore the room temperature anodic oxidation of GaAs is one of the preferred techniques for the fabrication of GaAs MOSFET's. The plasma oxidation which can also be performed at relatively low temperatures is essentially the same as wet anodic oxidation, except that the electrolyte is replaced by the plasma environment. The GaAs native anodic oxide can also be used in device processing, e.g., as a diffusion mask and also for device passivation. The anodic oxidation can be used as a precise etching process which can remove GaAs layers with a highly controlled thickness. An extensive effort has been carried out towards the better understanding of the complicated nature of the GaAs/oxide interface. Most of the experimental work in electrical characterization rely on the capacitance voltage (C-V) and conductance voltage (G-V) measurements under different bias, temperature and illumination conditions.

In this work, at first the surface properties of the semi-insulating, Cr doped GaAs substrates are investigated. The interface states energy distribution are studied using two beam TAV amplitude spectroscopy [47]. The studies include both oxidized and unoxidized GaAs surfaces. The oxides are grown using the wet anodic oxidation in a glycol and water based electrolyte [73]. The results reveal the presence of high density interface states in both cases (mainly acceptor levels at about 1 eV above the valence band) and the fact that the oxidation process increases the interface states density. The samples, oxidized at different current densities, are compared and those oxidized at lower current densities exhibit a

lower density of interface states. The physical models regarding the GaAs interface and oxidation mechanism are discussed by analyzing the experimental data. The GaAs:Cr unoxidized samples are also investigated at low temperatures using two beam TAV spectroscopy [85]. The characteristic exciton peaks are detected and the quenching of the exciton peak is observed upon shining the 1 eV bias light. The quenching effect which is attributed to the electron transition from the valence band to the high density interface states is not observed in semi-insulating, Fe doped InP [71]. The reason is attributed to the lower density of interface states in the upper half of the InP bandgap. A donor level at about 1.3 eV below the conduction band of GaAs which is only observable in oxidized GaAs samples at room temperature, becomes detectable in unoxidized GaAs at low temperatures.

The low resistivity GaAs samples are anodically oxidized under different oxidation current density waveforms [83,84]. The GaAs/oxide interfaces are examined by C-V measurements at different frequencies. The oxide bulk properties are compared by measuring such parameters as breakdown field and resistivity. The results indicate the superior interface properties at lower oxidation current densities and vice versa for oxide bulk properties. The analysis lead to an optimum current density waveform which starts at low values and after the termination of the nucleation and island growth phase [74] proceeds at a higher value of current density. The subjects to be discussed are classified as follows:

- Study of the semi-insulating GaAs surface and GaAs/oxide interface using two beam TAV spectroscopy [47],
- Quenching and enhancement of the exciton and subbandgap absorption in GaAs:Cr using two beam TAV spectroscopy at low temperatures [85],
- The effect of oxidation rate on the characteristics of Aℓ/anodic oxide/GaAs MOS structures [83,84].

5.1 Study of Semi-Insulating Cr Doped GaAs Surface and GaAs/Oxide Interface Using Two Beam TAV Spectroscopy

Semi-insulating GaAs is used as the substrate for LSI high speed digital circuits and microwave devices almost exclusively. The semi-insulating GaAs can be obtained by Cr doping and resistivities as high as 10^9 Ωcm can be achieved. Oxygen doping can also provide semi-insulating GaAs, but oxygen doped GaAs is not extensively used due to the high mobility of oxygen at processing temperatures. Undoped GaAs can also be used as a semi-insulating substrate, but its resistivity is smaller than Cr doped substrates. Although GaAs:Cr has been extensively studied in the past few years, the compensation mechanism and its variation under heat treatment are not well understood. The TAV measurements are especially applicable to the study of semi-insulating GaAs because of the high sensitivity of the TAV signal at low carrier concentrations. In this section the interface states energy level distribution of both unoxidized and oxidized GaAs:Cr samples are investigated.

5.1.1 Experimental Procedure and Results

The samples used in the following experiments are semi-insulating ($\rho > 10^7$ Ωcm), Cr doped, <110>, and polished at one surface. The oxidation is performed in a 3% aqueous solution of tartaric acid, buffered by NH_4OH to the pH = 5 and then mixed with propylene glycol in a 1:2 volume ratio [73]. This mixture which is called the AGW electrolyte provides a superior native anodic oxide as compared to completely aqueous [138] or non-aqueous solutions [139]. In AGW electrolyte, water is the oxidant and tartaric acid is used to increase the electrolyte conductivity. The pH is adjusted by NH_4OH. The addition of the propylene glycol to the aqueous solution drastically reduces the sensitivity of the oxidation process to pH variations and electrolyte contaminations. The reason is attributed to the less sensitive transport rate of the oxidizing species to the GaAs surface and the oxidation products from the GaAs due to the presence of the propylene glycol. The aqueous solution pH can vary between 2-9 in the AGW electrolyte, whereas it should be between 5-7 if the aqueous solution is used by itself. The dissolution rate of the native oxide in AGW is very small as compared to aqueous oxidation solutions ($\simeq 4 \times 10^{-2}$ A^o/sec and 1 A^o/sec respectively). By using AGW electrolyte, very uniform native oxides with high resistivity can be grown reproducibly.

The samples are oxidized at 0.1, 1.0 and 3.0 mA/cm^2, under constant current density regime. The oxidation cell consists of the GaAs:Cr anode, AGW electrolyte and platinum counter

electrode (cathode). The cell voltage is measured between GaAs and Pt electrodes. All the samples are oxidized until the cell voltage reaches the value of 50 volts, and then the current source is disconnected. At low current densities ($J < 1$ mA/cm^2), most of the voltage drop is across the growing oxide during the oxidation process and the ohmic drop across the electrolyte and thin GaAs samples are negligible. At higher current densities the voltage drop across the electrolyte and GaAs samples might not be negligible compared to the oxide voltage drop in the initial phases of the oxide growth (oxide thickness below 100 A^o). The GaAs samples are illuminated by a collimated white light during the oxidation. Therefore the holes that are needed for anodic oxidation are provided by photon absorption (samples are slightly n type in the dark). The illumination eliminates the extra voltage drop across the GaAs depletion layer which would have been otherwise needed in order to generate the oxidizing holes by avalanche process (breakdown voltage).

The cell voltage versus time curve at 0.1 mA/cm^2 current density is shown in Figure 5.1. This curve can be divided into two distinct phases. The first phase is the nucleation and island growth, followed by continuous oxide growth phase [74,76,140]. During the first phase the GaAs is not covered by the insulating oxide and the cell voltage is small and relatively time independent. After the complete coverage of the GaAs surface by anodic oxide, the second phase which is the continuous oxide growth starts. During this phase the cell voltage increases with time as the oxide thickness

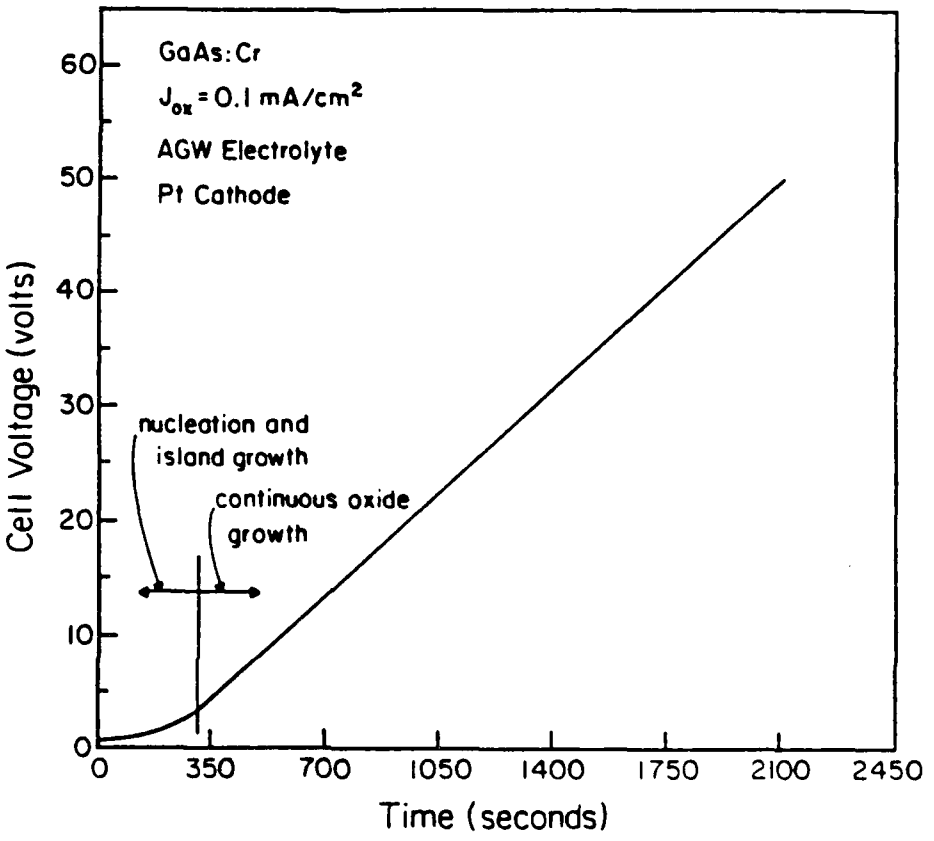


Figure 5.1 Oxidation cell voltage versus time curve for the semi-insulating, Cr doped GaAs sample, oxidized at 0.1 mA/cm^2 current density.

increases. The highly linear dependence of the cell voltage on time, indicates the oxide formation under constant electric field condition [75]. The oxide formation rate is about 10^{-4} cm/Col. considering the oxide electric field to be about 5×10^6 V/cm (oxide breakdown field). The average value of the oxide thickness per voltage drop across the oxide is 20 A^o/V. The nucleation phase is about 350 seconds long at 0.1 mA/cm^2 oxidation current density. The cell voltage versus time curves at higher current densities exhibit the same shape as the one shown in figure 5.1, except that the nucleation time is shorter and the slope of the linear region is higher (proportional to the current density). More discussions on the chemical nature of the oxidation process are presented in the following sections. Prior to oxidation the samples are cleaned with trichlorethylene, acetone and DI water. The native oxide is removed by HCℓ and rinses in methanol.

The interface properties of the unoxidized GaAs and oxidized GaAs are studied using two beam TAV spectroscopy. The delay line arrangement is as shown in figure 1.1a. The ground path is provided by an Aℓ film underneath the piezoelectric substrate. This arrangement is sufficient in these measurements because the surface potential modulation via an applied bias voltage is not needed (unlike the measurements in Chapters 3 and 4). A window is provided in the Aℓ film through which the surface under study of the samples can be illuminated by one or two monochromatic beams. The peak of the TAV waveform is recorded as a function of the incident photon

energy either manually or by using lock in amplifier and automatic scanning arrangement (for high resolution spectroscopy). The rf frequency of SAW is 110 MHz with the rf pulse width about 1 msec. The TAV waveform drops towards zero after the initial peak as shown in the inset of figure 5.2. The reason for this fast drop is the presence of the $LiNbO_3$ in the TAV detection path which introduces a small series capacitance. Therefore the time constant of the external circuit (τ_c in equation (3.39)) decreases and the TAV amplitude approaches zero after charging the capacitances. Since the TAV amplitude is measured at the peak, this effect does not cause any difficulty as long as the TAV peak reaches the steady state value, predicted by equation (2.40) ($\tau_{eff} < \tau_c$ in equation (3.39)). The TAV amplitude is a function of the near surface conductivity of GaAs and the GaAs/oxide interface as discussed in the previous chapters. In two beam spectroscopy, the wavelength of one beam is fixed (bias light, 750 nm = 1.65 eV, photon flux = 7×10^4/ cm^2 - sec), while the wavelength of the second beam (secondary light) varies between 500-2000 nm (both lights are simultaneously shone on the sample). The photon flux of the secondary light is kept constant by adjusting the input aperture of the monochromator. The secondary light photon flux is $7 \times 10^{14}/cm^2$ - sec for low power spectroscopy and approximately $3 \times 10^{15}/cm^2$ - sec for high power spectroscopy, in the following experiments.

The results of the TAV spectroscopy are shown in figures 5.2-5.4. Figure 5.2 shows the one beam spectroscopy of the

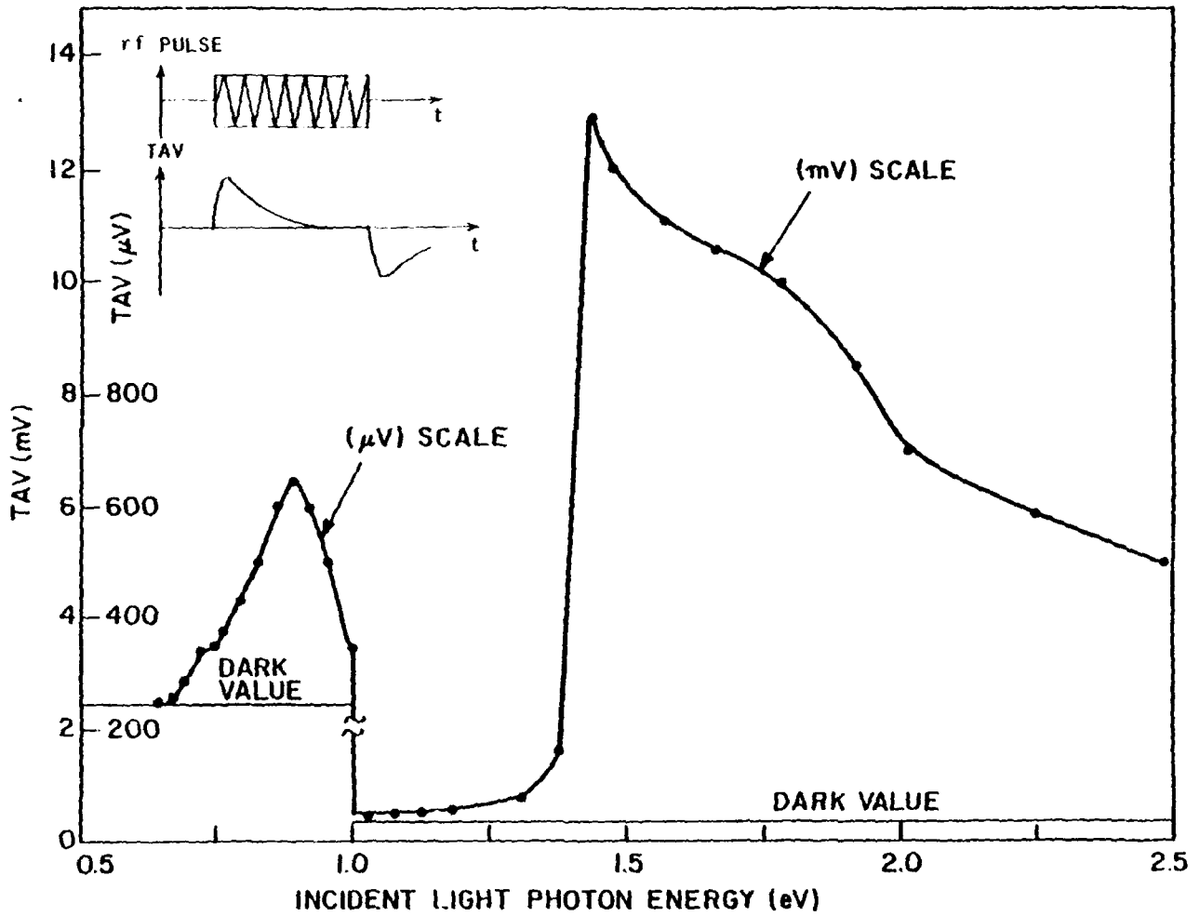


Figure 5.2 One beam TAV spectrum of the unoxidized, Cr doped GaAs. The incident beam photon flux = 7 x $10^{14}/cm^2$ sec.

unoxidized GaAs sample. In this figure, after the drop of the TAV amplitude under the sub-bandgap radiation (photon energy < 1.4 eV), a peak can be observed around 0.87 eV (≃ 1400 nm). This peak is much smaller than the bandgap peak (≃ 1/10). Except for the decrease of the TAV amplitude at photon energies larger than the bandgap, no other structure is detectable in the one beam spectrum. Figure 5.3 shows the two beam spectra of unoxidized and oxidized GaAs:Cr samples. In figure 5.3a the low power (secondary photon flux = $7 \times 10^{14}/cm^2$ - sec) two beam spectrum of the unoxidized GaAs:Cr is presented. A sub-bandgap minimum at around 1.05 eV can be observed. This minimum could not be detected using one beam spectroscopy (figure 5.2). It should be noted that the amplitude of the TAV is smaller than the bias light value at this minimum. Figures 5.3b,c,d present the low power two beam spectra of the samples, oxidized at 0.1, 1.0 and 3.0 mA/cm^2, respectively (secondary light photon energy is between 0.6-2.5 eV). In these spectra a stronger minimum around 1 eV can be observed (compared to figure 5.3a). A relative maximum around 1.25 eV is also present (below bias light value).

Figure 5.4 shows the high power two beam spectrum of all the samples for photon energies between 0.6-1.1 eV. The photon flux of the secondary light is increased by about a factor of 4, in order to reveal the sub-bandgap structure of the interface more clearly (photon flux ≃ $3 \times 10^{15}/cm^2$ - sec). In this figure, curve 1 is the spectrum of the unoxidized GaAs and curves 2, 3, and 4 correspond to the samples oxidized at 0.1, 1 and 3 mA/cm^2, respectively. The

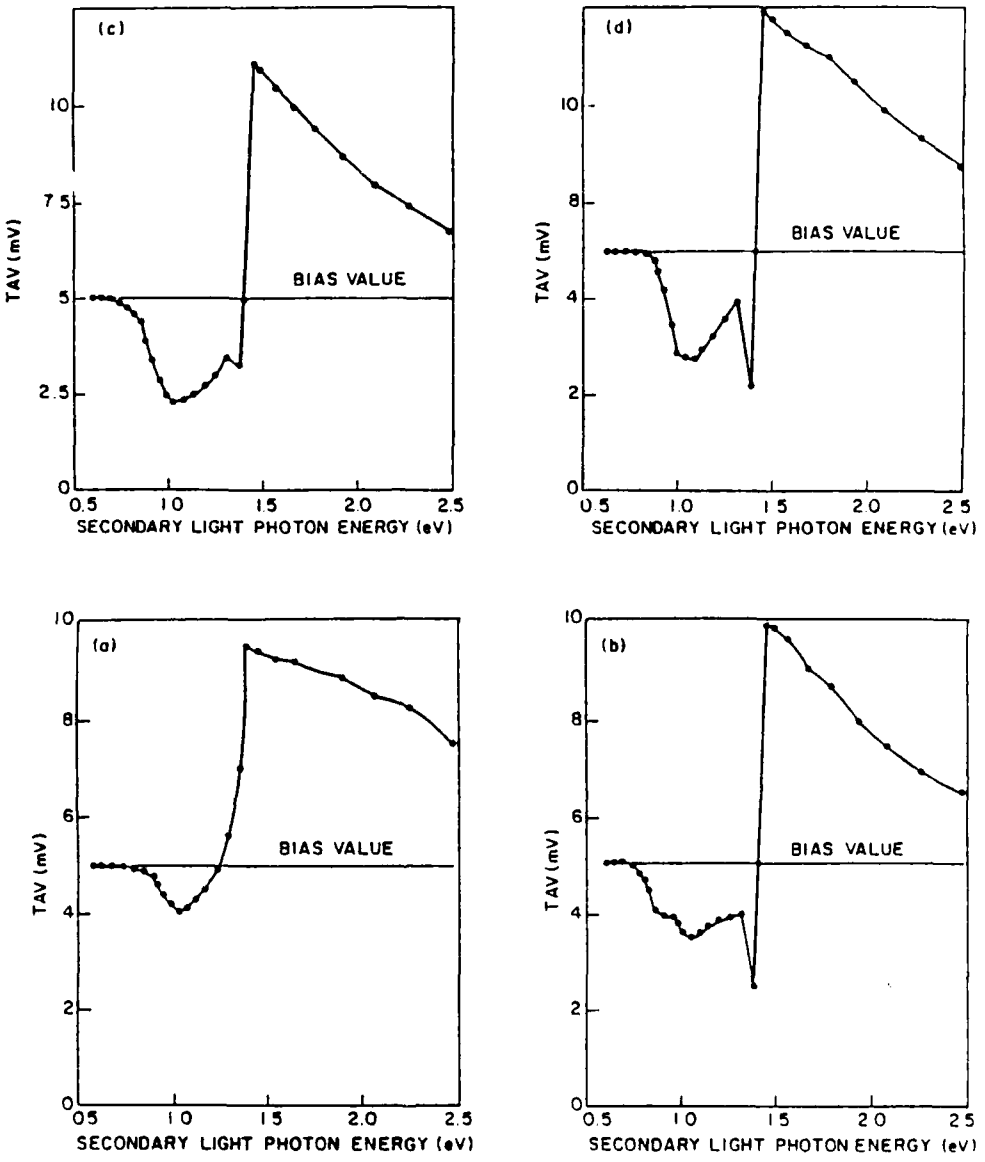


Figure 5.3 Low-power two-beam TAV spectra for the oxidized and unoxidized GaAs samples. The bias light photon flux = $7 \times 10^{14}/cm^2$ s, the bias light photon energy = 1.65 eV. The secondary light photon flux = $7 \times 10^{14}/cm^2$ s, the secondary light photon energy ~ 0.6-2.5 eV. (a) The unoxidized GaAs, (b) The GaAs oxidized at 0.1 mA/cm^2, (c) The GaAs oxidized at 1 mA/cm^2 and (d) the GaAs oxidized at 3 mA/cm^2.

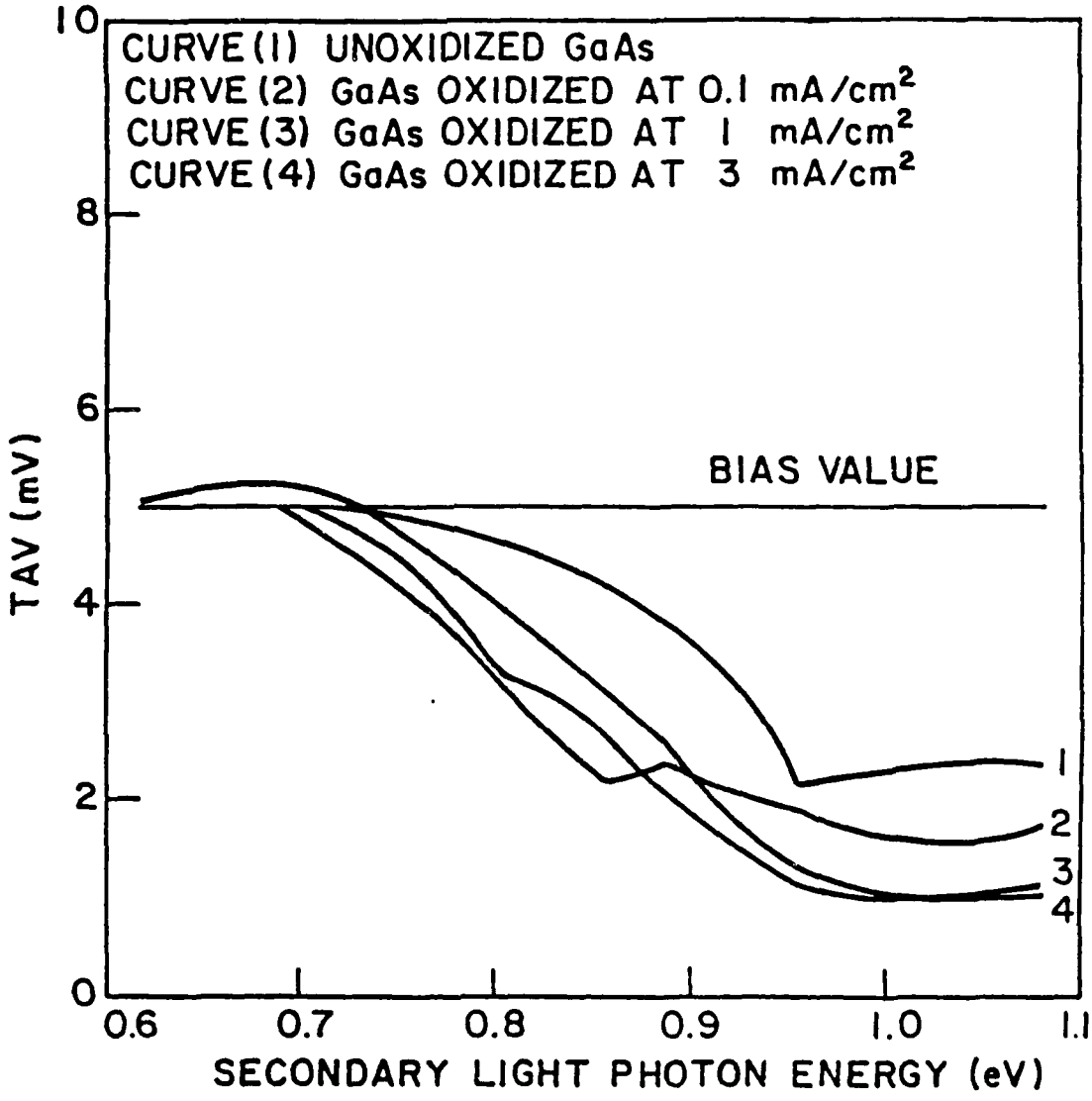


Figure 5.4 High-power two-beam TAV spectrum of the unoxidized and oxidized GaAs samples. The bias light photon flux = $7 \times 10^{14}/cm^2$ sec., the bias light photon energy = 1.65 eV. The secondary light photon flux = $2.8 \times 10^{15}/cm^2$ sec, the secondary light photon energy ~0.6-1.1 eV.

broad minimum around 1 eV energy can be observed for all the samples. The minima corresponding to the oxidized samples are stronger than the unoxidized sample. The samples oxidized at higher current densities (1 and 3 mA/cm^2) show stronger minima as compared to the one oxidized at lower-current density (0.1 mA/cm^2). The TAV amplitudes at 1 eV photon energy of the secondary beam, are shown in figure 5.5. TAV bias value is 5 mV for all the samples and a smaller TAV amplitude indicates a higher deviation from the bias value (stronger sub-bandgap transition). In figure 5.4, the GaAs, oxidized at 3 mA/cm^2 exhibits an additional peak at around 0.68 eV. The TAV amplitude at this maximum is larger than the bias value. This peak is not observed in the spectra of the other samples.

5.1.2 The Effect of Interface States on the Two Beam TAV Spectrum

For semi-insulating GaAs samples ($\rho > 10^7$ Ωcm, n type in the dark) the TAV amplitude is proportional to $(n\mu_n - p\mu_p)$ as discussed in equation (2.40). The theoretical plot of the TAV versus electron concentration is shown in figure 2.4. The difference between electron and hole surface photo-conductivities is monitored by the TAV amplitude.

The interface states are generally in one of the following forms:

A - Acceptor levels in the p or n semiconductor:

{ A-1 level below the E_f at dark,

A-2 level above the E_f at dark;

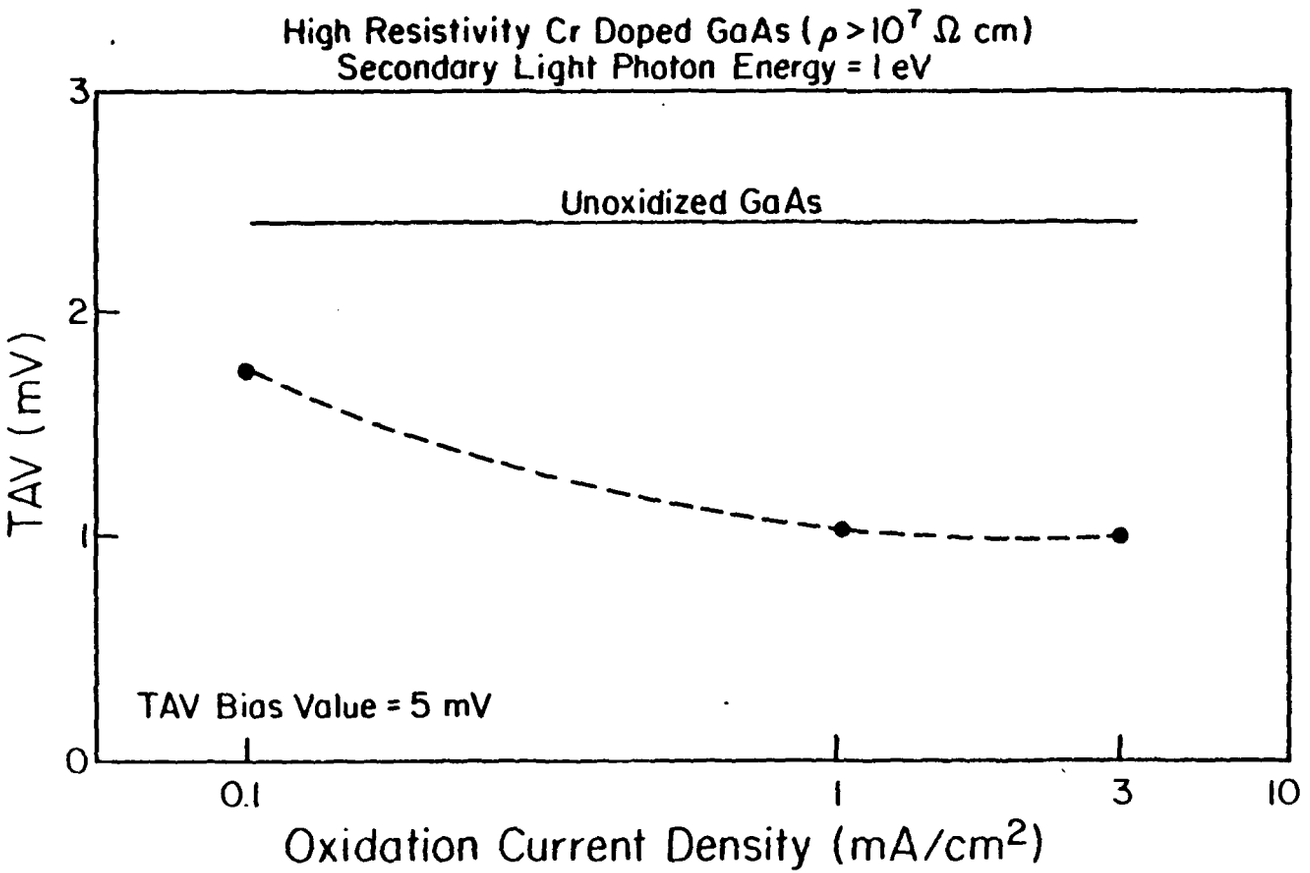


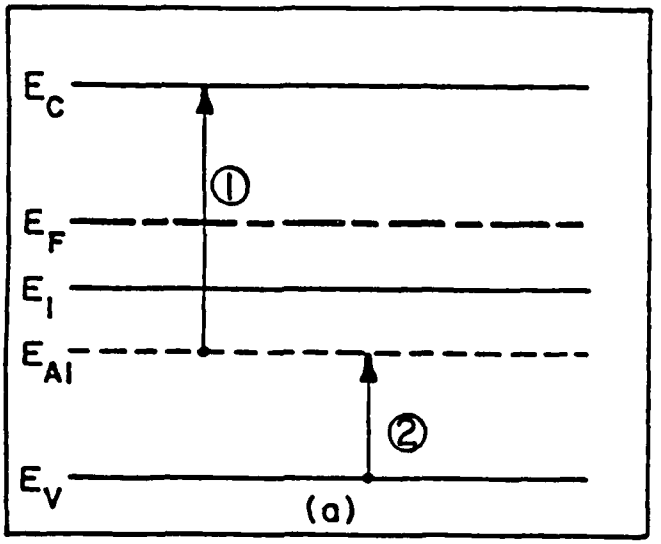
Figure 5.5 TAV amplitude at 1 eV photon energy of the secondary beam (high power) for unoxidized and oxidized GaAs:Cr samples. The smaller TAV amplitude indicates a stronger minimum (below bias value).

B - Donor levels in the p or n semiconductor:

{ B-1 level below the E_f at dark,
{ B-2 level above the E_f at dark.

Figure 5.6 shows the different cases of acceptor levels. For the case A-1, most of the available states (at energy E_{A1}) are filled up with electrons in the dark (figure 5.6a). In this case transition (1) is the electron transfer from the acceptor level to the conduction band and transition (2) is from the valence band to the acceptor level. Using one beam spectroscopy, the incident beam of energy $(E_c - E_{A1})$ should increase the TAV by enhancing the transition (1). The amount of increase is determined by the transition probability and the number of carriers available at E_{A1}. Incident beams of energy $(E_{A1} - E_v)$ do not change the TAV appreciably because the E_{A1} levels are mostly full. In the event of any effect the TAV should be smaller than the dark value due to the increase of the hole conductivity (if the sample is slightly n type in the dark such as GaAs:Cr samples). This effect is very small and practically undetectable for high resistivity samples.

By using the two beam spectroscopy in this case, the incident lights with photon energies between the bandgap value and $(E_c - E_{A1})$ have the following effect. The electrons are excited from the E_{A1} level to the conduction band. Therefore the states at E_{A1} become ready to accept electrons from the valence band, upon shining the secondary light with the $(E_{A1} - E_v)$ energy. This effect should cause a detectable decrease of the TAV below the bias value



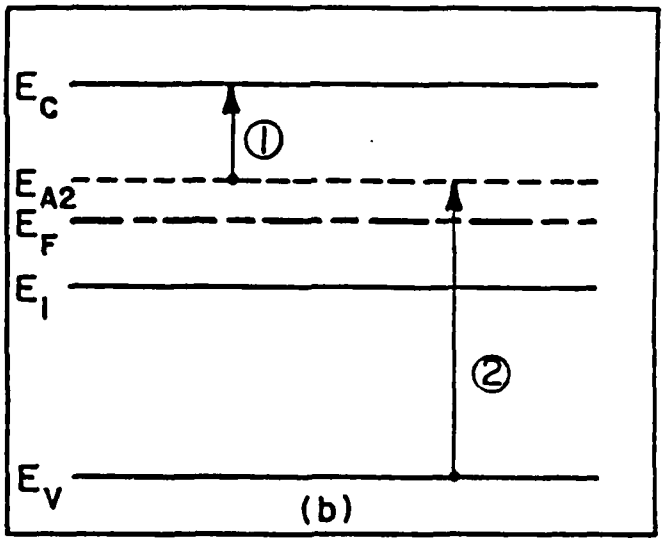


Figure 5.6 Transitions associated with a band of acceptor levels within the bandgap of an n-type semiconductor. a) The acceptor level (E_{A1}) is below the Fermi energy. b) The acceptor level (E_{A2}) is above the Fermi energy.

which determines the position of the acceptor level. This condition applies to CdS samples with two acceptor levels at around 0.8 and 1.3 eV above the valence band [45,71,95,96]. For the cases where the incident photon energy ($E_{A1} - E_v$) does not induce any other transition with opposing effect, the two beam spectroscopy is a very strong tool to detect the presence and the position of the acceptor levels below the Fermi energy [71].

The acceptor levels above the Fermi energy (E_{A2} in figure 5.6b) are mostly empty at the dark condition. Using one beam spectroscopy, the incident beam of energy ($E_c - E_{A2}$) does not have a strong effect on the TAV amplitude due to the small number of available electrons at the E_{A2} level (transition (1)). The electron transfer from the valence band to E_{A2} (transition (2)) should quench the TAV amplitude by increasing the hole conductivity. Due to the small dark value of the TAV amplitude for high resistivity GaAs (point A in figure 2.4), the quenching effect of transition (2) is very weak and undetectable (unless a surface inversion by the incident beam is possible). The two beam illumination in this case causes a large TAV by the bias light with the photon energies greater than or equal to the bandgap (point B in figure 2.4). The secondary incident beam with energy ($E_{A2} - E_v$) decreases the TAV amplitude below the bias value (point C in figure 2.4). The quenching effect of transition (2) can be easily detected in this condition. This condition applies to the TAV spectra of GaAs samples that are presented in figures 5.2-5.4. The donor interface

states can also be monitored similarly. The effects of transitions (1) and (2) (figure 5.6) on the TAV amplitude are directly proportional to the density of the interface states. For the semiconductors exhibiting the same interface states energy levels, the density of these states can be compared by the comparison of the TAV spectra. The capture and emission rates of the interface states can be measured by interrupting the secondary light and monitoring the TAV amplitude variation as a function of time, as it changes from the two beam steady state value to its bias value.

5.1.3 Discussion of the Experimental Results

The presented data can be analyzed as follows: (1) The weak maximum around the 0.87 eV in the unoxidized sample spectrum (figure 5.2) is believed to be due to the Cr level which is an acceptor level located at 0.87 eV below the conduction band as shown in figure 5.7. The transition of the electrons from the Cr level to the conduction band increases the TAV slightly (transition (3) in figure 5.7). Transition (4) is weak and cannot be detected due to the small number of available states in the Cr level (Cr levels are mostly filled because they are below Fermi level). Except for the sharp TAV drop at the sub-bandgap radiation, the only other feature in this spectrum (figure 5.2) is the decrease of the TAV amplitude at photon energies larger than the bandgap. This feature which is common in all the presented spectra, is due to the effect of the surface recombination. At a fixed surface recombination

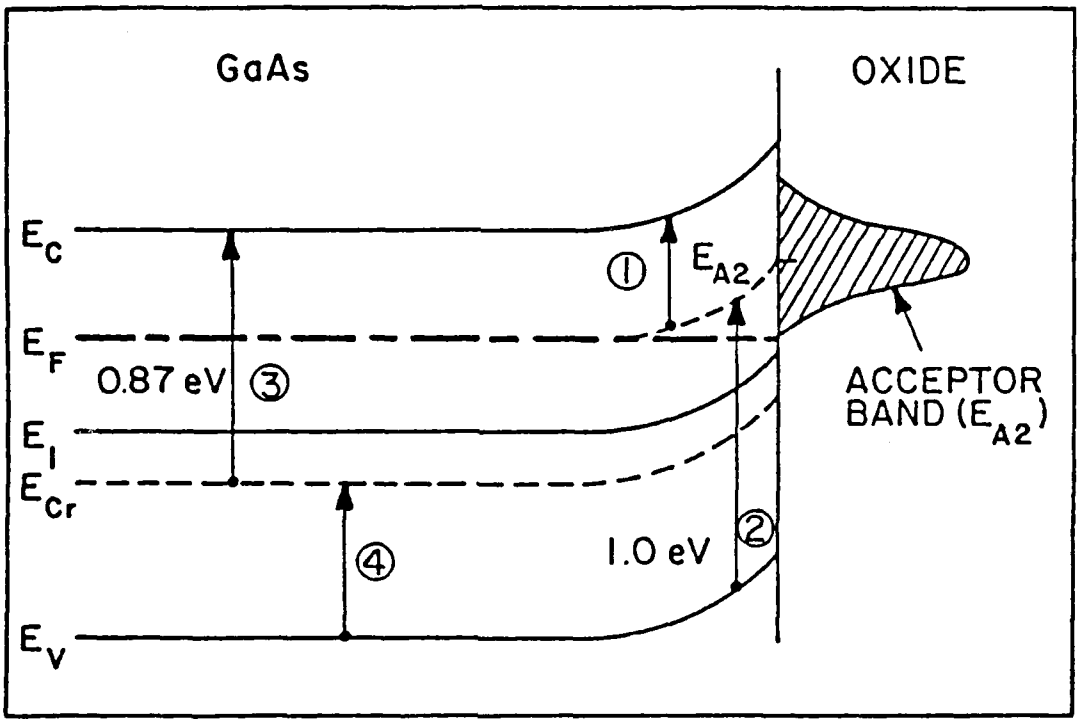


Figure 5.7 The interface band structure of the GaAs and the GaAs/anodic oxide interface.

velocity the recombination rate of the photogenerated carriers increases if they are generated closer to the surface. The photons with energies higher than the bandgap are absorbed closer to the surface because of the higher absorption coefficient. Therefore the photo-generated carriers (at higher than the bandgap energies) exhibit a higher recombination rate and the TAV amplitude decreases. It should be noted that by the equal generation of electron and holes, the TAV amplitude goes up due to the higher mobility of electrons (TAV α $n\mu_n - p\mu_p$).

(2) The broad minimum at around 1 eV which is observed in the two beam spectrum of the unoxidized sample (figure 5.3a) is attributed to a high concentration of deep acceptor interface traps centered around 1 eV above the valence band. These levels are shown in figure 5.7 (E_{A2} levels). The excitation of electrons from the valence band to these acceptor levels (transition (2) in figure 5.7) decreases the TAV amplitude below the bias light value. It should be noted that this minimum is not detectable in the one-beam spectrum.

(3) Figures 5.3b,c,d show the two beam spectra of the GaAs samples, oxidized at 0.1, 1 and 3 mA/cm^2 respectively. It can be seen that the minimum around 1 eV is present for all the oxidized samples. This minimum is stronger than the unoxidized sample. This effect is due to the oxidation process which causes a higher density of E_{A2} acceptor traps. There is also a relative maximum at around 1.25 eV which is only observable in oxidized samples. These maxima

are attributed to the donor-like interface traps which are centered at about 1.25 eV below the conduction band. The possible origins of the observed acceptor and donor levels will be discussed shortly. The maxima at around 1.25 eV can also be observed in unoxidized GaAs samples, but only at low temperatures, as will be shown in section 5.2.

(4) To compare the density of states for the samples oxidized at different current densities, the high power two beam spectroscopy is performed in the range of 0.6 - 1.1 eV. The results are shown in figure 5.4. The comparison of the spectra clearly reveals the increase of the interface states density for the samples oxidized at higher current density. Curve 2 corresponds to the sample oxidized at 0.1 mA/cm^2 which shows a minimum, stronger than the unoxidized sample (curve 1) but weaker than the samples oxidized at 1 mA/cm^2 (curve 3) and 3 mA/cm^2. Curve 4 exhibits a peak at the photon energy of $\simeq$ 0.67 eV. This peak (above the bias light value) is due to the transition of the electrons from the E_{A2} band to the conduction band (transition (1)). The effect of this transition can only be observed when the interface states density at the E_{A2} is high enough to induce a detectable change in the TAV signal. It should be noted that in some cases the position of the peaks are shifted towards the higher energies. This effect can be due to the momentum transfer needed, in addition to the supply of the energy difference between levels, in order to induce the band to acceptor level transition. Another reason can be due

to the high density of closely spaced acceptor levels (band like) which can broaden the TAV peaks. From the data presented, it can be concluded that: (a) A high density of deep acceptor interface traps, centered around 1 eV above the valence band, are present in the unoxidized GaAs samples. (b) These acceptor levels also exist at the GaAs/oxide interface with a higher density. (c) The density of states increases if the samples are oxidized at a higher current density. (d) Donor levels centered around 1.25 eV below the conduction band can be detected only in the oxidized samples spectra.

5.1.4 Discussion on the Anodic Oxidation Mechanism and GaAs Interface States

As shown in figure 5.1 the oxidation process can be divided into two distinct phases. The oxidation mechanism during these phases can be explained as follows.

Phase (a): The nucleation and island growth. The oxidation starts by nucleation process and then proceeds by the two dimensional growth of the oxide from the nuclei centers [74]. By ESCA (electron spectroscopy for chemical analysis) investigation of the chemical nature of the oxide during this initial phase, it is shown [76,140] that the oxide primarily consists of Ga_2O_3 with indications of excess elemental As at the interface (oxide thickness below 40 A^o). This analysis is confirmed by other workers using Auger or ESCA depth profiling of the fully grown oxide [141,142]. Although this is not a unique result, reported in the literature (especially the presence of the elemental As at the GaAs/oxide

interface) it seems to be the most reliable one. The reasons for th lack of As_2O_3 in the oxide at the initial oxide growth phase and the presence of elemental As at the interface can be as follows:
(1) Preferential oxidation of Ga_2O_3 as compared to As_2O_3. The reaso is the higher free energy of formation of Ga_2O_3 ($\simeq$ -230 K cal/mole) compared to As_2O_3 ($\simeq$ -140 K cal/mole). (2) Dissociation of the As_2O in the presence of GaAs into elemental As and Ga_2O_3, while Ga_2O_3 is stable. The reason is that the reaction 2 GaAs + As_2O_3 $\rightarrow$ Ga_2O_3 + 4 A is exothermic while 2 GaAs + Ga_2O_3 $\rightarrow$ As_2O_3 + 4 Ga is endothermic [14 (3) As will be discussed later, the oxidation process most probably proceeds by the transport of Ga and As ions through the oxide to the oxide/electrolyte interface (under the influence of the electric field). The energy barrier height encountered by As ions during the transport is higher due to the larger As ionic radius as compared to Ga [142] (0.69 and 0.62 A^o respectively). (4) The As oxides are more soluble in water than Ga oxide (Ga_2O_3 is insoluble in water). Therefore the As oxide might leave the thin oxide island as it is formed [76]. Some of the experiments performed by using high concentrations of As oxides in the electrolyte did not showan appreciable difference in the chemical composition of the initial thin oxide [140]. Thus, this might not be the dominant effect in determining the chemical composition of the GaAs/oxide interfacial region (not the case for oxide bulk). It is shown that the oxidation current density affects the structure of the Ga_2O_3 layer which is formed in this phase [77,143]. Higher oxidation current density

(> 1 mA/cm^2) produces a crystalline structure (β Ga_2O_3, [77]), while the Ga_2O_3 transition layer is amorphous at lower current densities. The crystallization is also observed at lower current densities if the samples are annealed at temperatures above 500° C. Thus the higher oxidation current densities (> 1 mA/cm^2) can produce a transition region between the GaAs and the oxide bulk which contains β Ga_2O_3 crystallites and is relatively porous. It is also postulated that during the oxidation process, oxygen vacancies are produced at the GaAs/oxide interface [142] which result in a high defect concentration. In this case a higher oxidation current density produces a larger defect concentration and therefore a higher interface state density.

Phase (b): Island coalescence and continuous oxide growth. This phase starts after the GaAs surface is fully covered by a thin oxide layer (mostly Ga_2O_3), due to the coalescence of the oxide islands. During this phase the oxide thickness increases while the electric field is constant within the bulk of the oxide. This effect is demonstrated by the highly linear portion of the curve in figure 5-1 (under constant current density). The mechanism of the ionic transport through the oxide in this phase is still speculative to some degree. The most agreed upon mechanism is the transport of the Ga and As ions through the oxide and their anodic reaction with oxygen near the oxide surface. The concentration of the As_2O_3 is much higher in the bulk of the oxide than the thin interfacial region. The Ga to As ratio is about 1.8 in the bulk of

the anodic oxide [141,142]. The higher concentration of As_2O_3 improves the oxide bulk properties with respect to such parameters as oxide resistivity and breakdown field. The thermally grown GaAs native oxides are almost completely composed of Ga_2O_3 [144]. These oxides exhibit a low resistivity ($\rho \simeq 10^{10}\ \Omega$ cm) and low breakdown field ($\simeq 2 \times 10^5$ V/cm). As will be shown later, the anodic oxides with resistivities higher than $10^{14}\ \Omega$ cm and breakdown fields in excess of 5×10^6 V/cm can be grown reproducibly. The optimum GaAs ratio for the best oxide bulk quality is not clearly determined, but it seems that the ratio of 1.8 which corresponds to equal volumes of Ga_2O_3 and As_2O_3 is the most stable composition. The As_2O_3 concentration drops near the surface of the oxide and the Ga/As ratio is about 3 in this region [141]. This effect should be due to the solubility of the As oxide in the water. By using a higher current density in this phase, the oxidation rate can be increased, which shortens the oxidation time needed for a certain oxide thickness. Therefore higher current densities can cause a higher concentration of As_2O_3 in the oxide bulk which leads to a better oxide bulk quality. Shortening the oxidation time also decreases the density of contaminents and water related traps in the oxide. This effect will be experimentally demonstrated in the following sections.

The exact source of the different interface traps at the GaAs surface are not known at the present time. The GSCH model [80] and the work by Panday [81] can be used to explain the acceptor levels present at the unoxidized GaAs surface. The surface

electronic states are calculated for ideal (no surface bond relaxation) and relaxed GaAs surfaces using the semi-empirical tight binding method (SETB) [81]. The ideal surface only exhibits the discontinuity of the crystal structure with no change in the Ga-As bond length or angle. In the relaxed surface the Ga-As bonds make an angle (tilt angle) with the corresponding bonds of the ideal surface (bond lengths are not altered). The calculated electronic states (in some cases compared with the photo-emission spectroscopy data) commonly exhibit two peaks, one near the top of the valence band, and the other near the bottom of the conduction band. The decomposition of localized states into their orbital components, indicate that these peaks are mainly due to filled and empty As-P and Ga-P orbitals respectively [81]. In the GSCH model it is considered that, due to the difference between the Ga and As potentials, there is an electronic relaxation of dangling bands [80]. The As surface atoms acquire an electron and form the filled surface states (near the valence band), and the surface Ga atoms lose the electron of their dangling bond and form the localized empty surface states (near the conduction band). Therefore according to both of the above models the filled and empty surface states are associated with and localized on the column V and III atoms respectively. The acceptor levels centered around E_{A2} ($\simeq$ 0.4 eV below conduction band) which are detected in the two beam TAV spectroscopy of unoxidized samples are attributed to the Ga-P empty orbitals.

The anodic oxidation produces an interfacial region between the GaAs bulk and the oxide bulk. This region with a thickness on the order of 100 A^{o} is disordered, highly non-stoichiometric, and contains a high defect density as discussed earlier. It is proposed that due to the high density of defects at the interface, they are no longer localized two dimensionally [78,79]. Therefore they constitute a high density interface state band (ISB) which is U shaped with increasing density in the upper half of the bandgap. The wave functions of the states within this band overlap at certain energies, within which, the state to state transitions are frequent. In this model the carriers are exchanged between GaAs bands and ISB by tunneling through the interfacial region. The trap density exponentially decays as a function of depth into the oxide. The traps closer to interface exchange carriers very rapidly, while the further traps are slow. This model has been successful in explaining the anomalous frequency dispersion of the accumulation capacitance of the anodically oxidized n-GaAs samples [78]. Other observed properties of the GaAs/anodic oxide system such as the oxide traps charging effect (injection type hysteresis) can also be explained by this model. These effects will be experimentally investigated as a function of oxidation current density, in the following sections. The oxidation current density can affect the composition and crystal structure of the interfacial region. As discussed earlier, higher current densities can produce a higher density of interface defects by forming β Ga_2O_3 crystallites and possibly oxygen vacancies.

The presence of the ISB acceptor band is detected by the two beam TAV spectra for the oxidized samples. It is shown that the density of this band is indeed higher than in the unoxidized sample and a larger oxidation current density produces a higher interface trap density (figure 5.4, 5.5). Since the acceptor traps exist in both oxidized and unoxidized samples, this implies the intrinsic nature of the GSCH model due to GaAs surface discontinuity. Anodic oxidation aggrivates the situation by introducing a highly nonstoichiometric interfacial region with a high defect density. The defects can extend two dimensionally in the interfacial plane in order to form non-localized electronic states. Under this condition the interface states band (ISB) is formed as opposed to localized state continuum. In localized state continuum (such as in Si), the energy levels are so closely spaced that they cannot be resolved individually, but due to spatial localization the wave functions do not overlap and the electronic states are non-interacting.

The time constant associated with transition (1)(figure 5.7) is measured by interrupting the secondary light while monitoring the TAV amplitude variation between steady state values (this transition causes the 0.67 eV peak in figure 5.4). A long time constant (on the order of five minutes) is observed for this transition which is attributed to the carrier exchange by tunneling between the E_{A2} level and the conduction band. The relative maximum observed around 1.25 eV in figures 5.3b,c,d can be due to the donor levels which are enhanced by the increased defect density in the interfacial

region, due to the oxidation, as pointed out in [82]. Although the samples used in the above measurements are high resistivity GaAs samples, the experimental conclusions and discussions on the oxidation mechanism and interface trap levels are general and they apply to both p and n, high and low resistivity GaAs samples. The experimental results on low resistivity samples are presented in section 5.3.

5.2 Quenching and Enhancement of the Exciton and Sub-Bandgap Absorption in GaAs:Cr Using Two Beam Spectroscopy at Low Temperature [85]

The exciton absorption or emission causes a sharp peak at the energies lower than the main band to band transition (direct gate at k=0) in GaAs, as observed in the optical absorption [88-a] and photoluminescense [88-b] spectra. The excitonic effect has also been detected, using the electro-reflectance technique [89]. Excitonic states are created when a free electron and a free hole are attracted by Coulomb interaction and form a bound electron hole pair. In a semiconductor crystal the electrons and holes interact strongly at low temperatures, at which their kinetic energy is low enough to allow them to form a bound state. Exction particles are analogous to hydrogen atom with the nucleus replaced by a hole. The exciton binding energies can be calculated to a good approximation, using the hydrogen atom model. This binding energy is about 100 to 1000 times smaller than the hydrogen atom for the following reasons. First the reduced mass of the electron-hole system should be used in this model and second the dielectric constant of the crystal should

be considered instead of the vacuum dielectric constant. Exciton binding energies also exhibit the ground state (n=1) and higher excitation states (n=2,3,...). Exciton states are more detectable in a pure semiconductor with higher resistivity and lower defect concentration. The reason is that at high carrier concentrations the Coulomb interaction is screened by the free carrier, therefore reducing the bound electron-hole pair concentration. The simple form of excitons, created by interaction between free carriers, is called the free excitons. The interactions between free carriers and other particles such as ionized donors or acceptors form the bound excitonic states. The theoretical treatments and experimental implications of various exctionic states constitute a very interesting and increasingly important field of solid state physics. For a detailed discussion of exciton characteristics and their applications, see [86] for example.

In this section the one and two beam TAV spectroscopy at low temperature is used to study the excitonic effect and the quenching and enhancement of the exciton peak by a monochromatic bias light [85]. Another sub-bandgap structure is observed at around 1.3 eV photon energy of the secondary beam. This structure which is only observable at low temperature, also exhibits the quenching effect. The obtained data are used to delineate the GaAs interface level energy distribution (which also confirm the results obtained in the previous section). Another property of the semi-insulating GaAs (GaAs:Cr or GaAs:O) which is the persistent quenching of the photo

conductivity [90-92] or optical absorption [93] at low temperatures, is also analyzed based on the experimental data.

5.2.1 Experimental Results

The experimental arrangement is the same as in the previous section except for the following. 1) The TAV amplitude is measured by lock in amplifier and the spectra are recorded automatically as a function of secondary light wavelength. 2) A high resolution monochromator is used as the scanning beam (secondary beam) with the resolution of about 5 A^{o} in the desired scanning range (8000-10000 A^{o}). One beam spectra of the GaAs:Cr samples are shown in figure 5.8. The room temperature spectrum shows the direct band to band transition at 1.432 eV with almost no additional structure. The spectrum at 193^{o} K exhibits a sub-bandgap peak with a half width of about 0.005 eV, positioned before the bandgap absorption edge at 1.468 eV. This peak is associated with free excitons at ground state (n=1). At lower temperature (93^{o} K) in addition to the exciton peak, another maximum can be detected at around 1.3 eV. It should be noted that in all cases the TAV amplitude is directly proportional to the conductivity difference between holes and electrons. Also TAV is smaller at low temperatures due to the lower number of free carriers (different scales in figure 5.8). The amplitude of the exciton peak is dependent on the scanning direction of the incident beam wavelengths, as shown in figure 5.9. The peak is stronger for the scan direction from high to low photon energies.

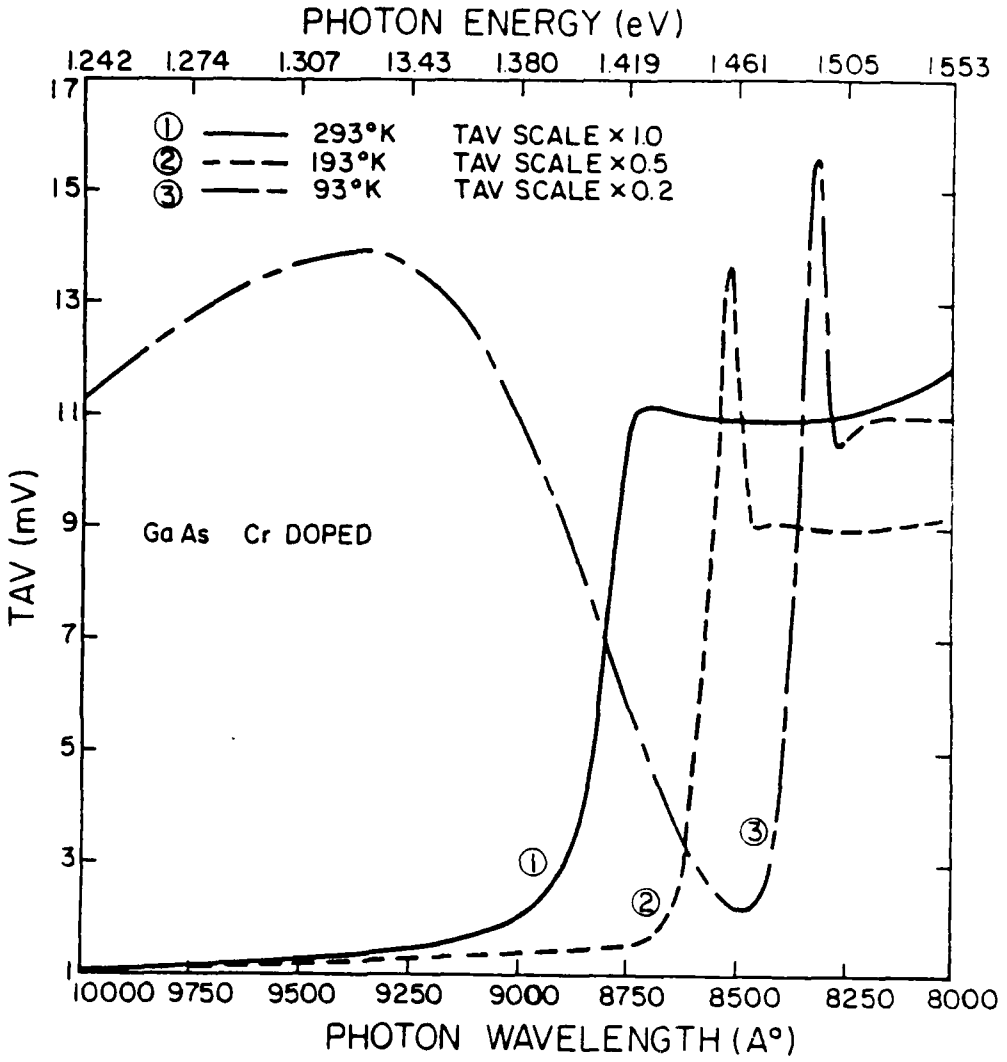


Figure 5.8 One beam TAV spectra of the GaAs:Cr at 293°K, 193°K and 93°K, exhibiting the exciton peak and sub-bandgap structures at lower temperatures.

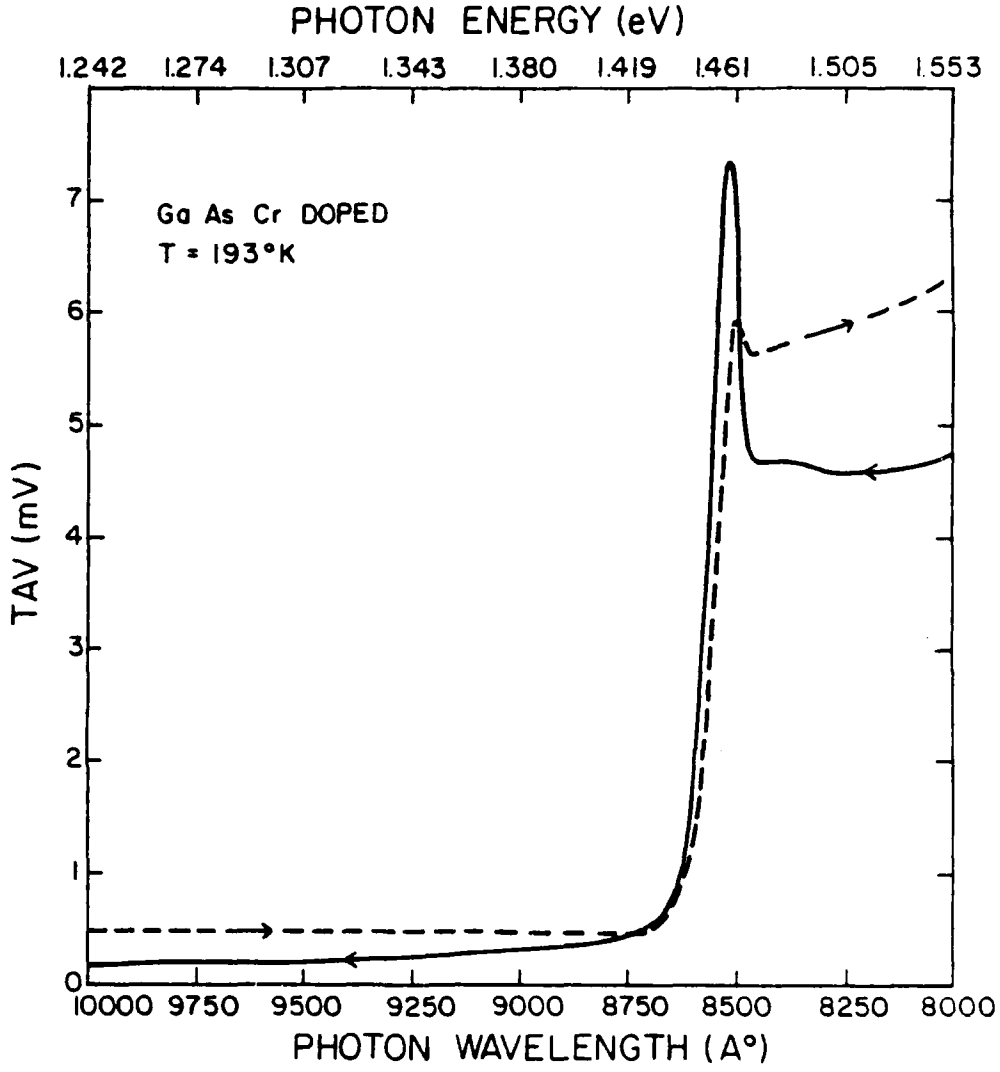


Figure 5.9 The effect of the direction of the scanning beam on the exciton peak in GaAs:Cr.

The effects of bias light at two different wavelengths, along with the one beam spectrum are shown in figure 5.10 (temperature = 98° K). The demonstrated bias wavelengths correspond to enhancement and quenching conditions and they are fixed for each of the TAV spectra. The bias light is provided by a monochromator with a lower resolution (on the order of 50 A°) than the scanning beam monochromator. It is shown that the bias light at 900 nm (≃ 1.38 eV) enhances the excitonic peak. It should be noted that the TAV amplitude is increased at all the wavelengths under this bias light, but the increase at the wavelengths corresponding to the exciton peak is stronger. The bias light at 1250 nm (≃ 1 eV) completely quenches the exciton peak and the 1.3 eV maximum. This effect is very strong and is indicative of a strong sub-bandgap transition, induced by the bias light. In this case the amplitude decreases at all wavelengths of the scanning beam, indicating an increase of the hole conductivity. The effect of bias lights with wavelengths in between the above wavelengths and shorter than 900 nm are as follows (not shown in figure 5.10). At bias wavelengths both longer and shorter than 1250 nm the quenching effect decreases. Going from 1250 nm towards 900 nm, the quenching effect diminishes (at around 1000 nm) and for wavelengths shorter than 1000 nm, the enhancement effect starts. The enhancement effect peaks at slightly below 900 nm (at around 1.3 eV) and then decreases by moving towards bias light with bandgap energy (≃ 825 nm). At bias light wavelength of 820 nm (higher than bandgap energy) a small exciton

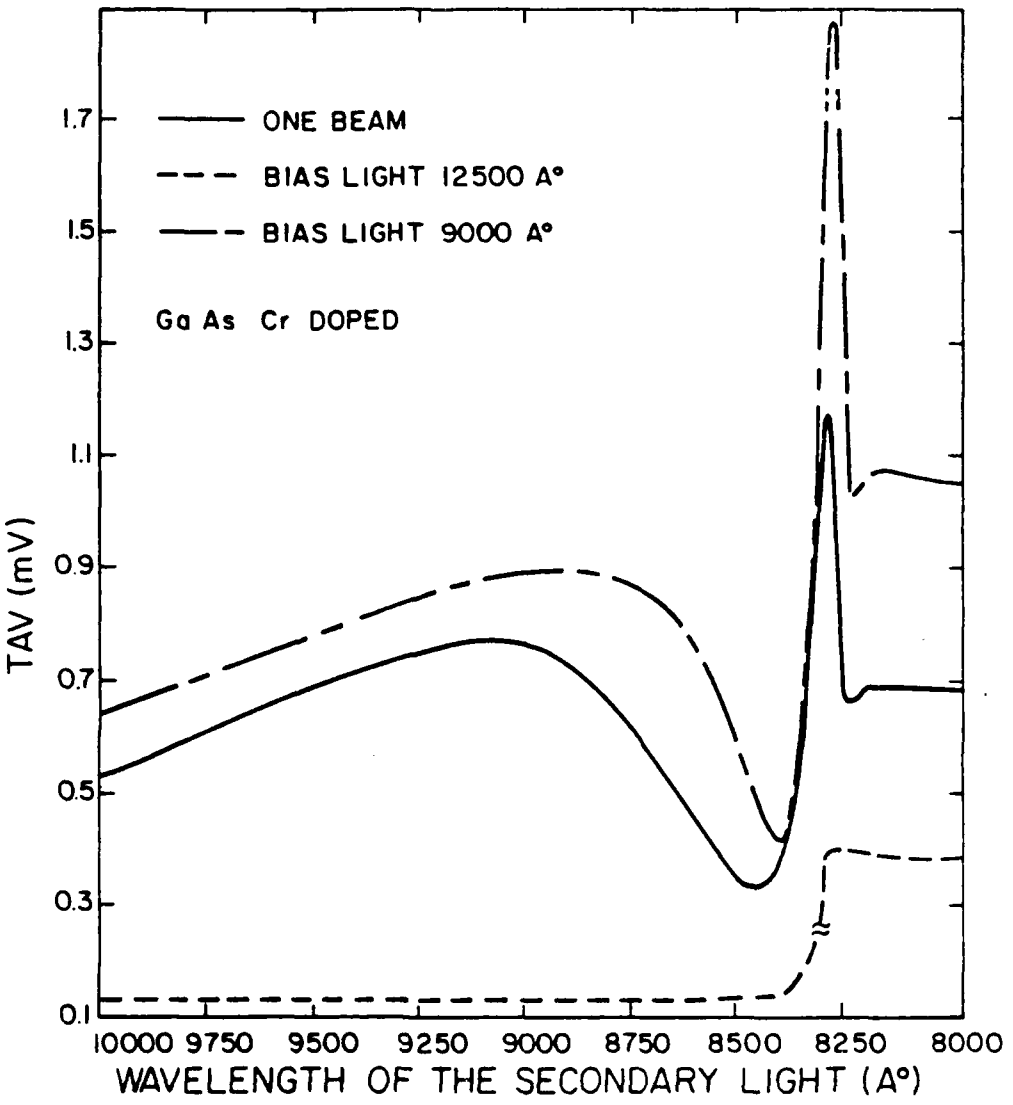


Figure 5.10 The quenching and enhancement effects, shown by the two beam TAV spectra of the GaAs:Cr at 98°K using 12500 A° and 9000 A° bias light.

quenching effect is observed, even though the overall TAV amplitude at other wavelengths is increased. In all of the above analysis, the quenching, enhancement and variations of TAV spectra are observed in comparison with the one beam spectrum.

5.2.2 Discussion of the Results and Quenching and Enhancement Effects

The theoretical model which explains the presented data is as follows.

(1) The TAV peak at about 1.3 eV which is shown in figure 5.8 for 93^{o} K is attributed to a band of donor levels around 1.3 eV below the conduction band (E_{D1}). Due to the slightly n type nature of the GaAs:Cr, this donor band is filled in the dark. The 1.3 eV illumination excites the electrons from this band to the conduction band, thus increasing the electron conductivity and the TAV amplitude. This donor band was predicted in the previous section [47]. One reason that the E_{D1} level is detectable only at low temperatures (93^{o} K in figure 5.8) is the decrease of the free carrier concentration, which is over shadowed by the stronger signal due to the electron excitation from the E_{D1} level to the conduction band. Another reason canbe due to the shift of the filled As electronic states [80,81] from below the valence band maximum into the bandgap region, caused by lowering the temperature. This level which is not observable at room temperature for unoxidized GaAs, becomes detectable upon oxidation (section 5.1.3), suggesting that the oxidation increases the density of E_{D1} levels [82].

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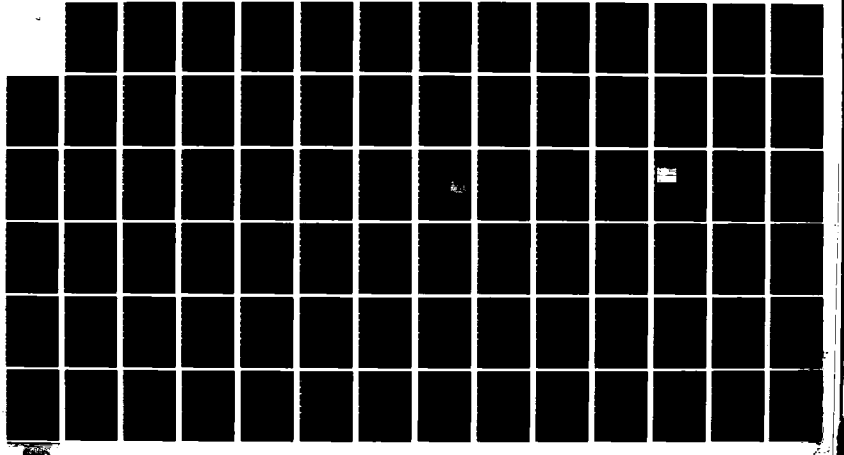

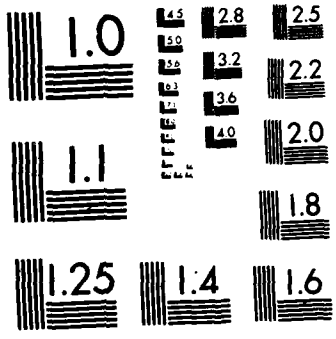

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(2) The exciton peak observed in figure 1 (93^{o} K and 193^{o} K) is due to the dissociation of free excitons into free electrons and holes. Because of the higher mobility of electrons, the net effect is the increase of the TAV amplitude. The excitonic absorption process can be discussed in more detail as follows. The bound electron-hole pairs which constitute the free excitons are created upon illumination with higher energies than ($E_g - E_x$) where E_g is the bandgap and E_x is the free exciton binding energy at ground state ($\simeq$ 5 meV). The excitons can be formed at higher energies than the bandgap because they can be created with some kinetic energy. In all the spectra presented in this section (except for the dashed one in figure 5.9) the direction of the scanning beam is from high to low photon energies. Therefore at energies higher than $E_g - E_x$ the excitons are created at low temperatures (see for example curve (2) in figure 5.8). A quasi steady state is reached between the excitonic state density and free carrier concentration at incident beam energies above the bandgap or more precisely, above $E_g - E_x$ (quasi-steady state, because the wavelength and thus the absorption coefficient are varying). After the incident photon energy falls below $E_g - E_x$, the concentration of excitons drop to a lower value. The exciton annihilation takes place by the recombination or exciton ionization into free carriers [145,87]. The exciton ionization which can take place under the influence of the electric field, produced by the SAW nonlinear interaction, gives rise to the exciton peak which is observed in

the TAV spectra. Thus a high exciton recombination rate can quench the exciton peak (the effect of exciton ionization into free carriers is reduced). The large sensitivity of the exciton peak to the direction of the photon energy scan (figure 5.9) is due to the fact that the created exciton density is much lower for the scan direction from low to high energies.

The very strong quenching effect of the exciton peak upon shining the bias light with 1250 nm wavelength (≃ 1 eV, figure 5.10) is attributed to the electrons transition from the valence band to the acceptor level centered around 1 eV above the valence band (E_{A2}). This acceptor level was also detected previously [47] by the minima that it introduced in the two beam TAV spectra (discussed in the previous section). The electron transition from valence band to E_{A2}, increases only the hole concentration and has the following effects. 1) The exciton peak almost completely disappears due to the increase of the exciton recombination rate. 2) The TAV amplitude decreases at all wavelengths because of higher hole conduction (TAV α $n\mu_n - p\mu_p$). The low temperature TAV spectroscopy of semi-insulating Fe doped InP is also performed [71]. One beam TAV spectra at different temperatures are shown in figure 5.11. The exciton peak can be observed at low temperatures without any additiona sub-bandgap structure in the scanned range. Two beam spectroscopy at different bias light wavelengths are also performed. The results do not show any appreciable quenching or enhancement effects, suggesting the lower density of interface states, as compared with GaAs. The elimination of the

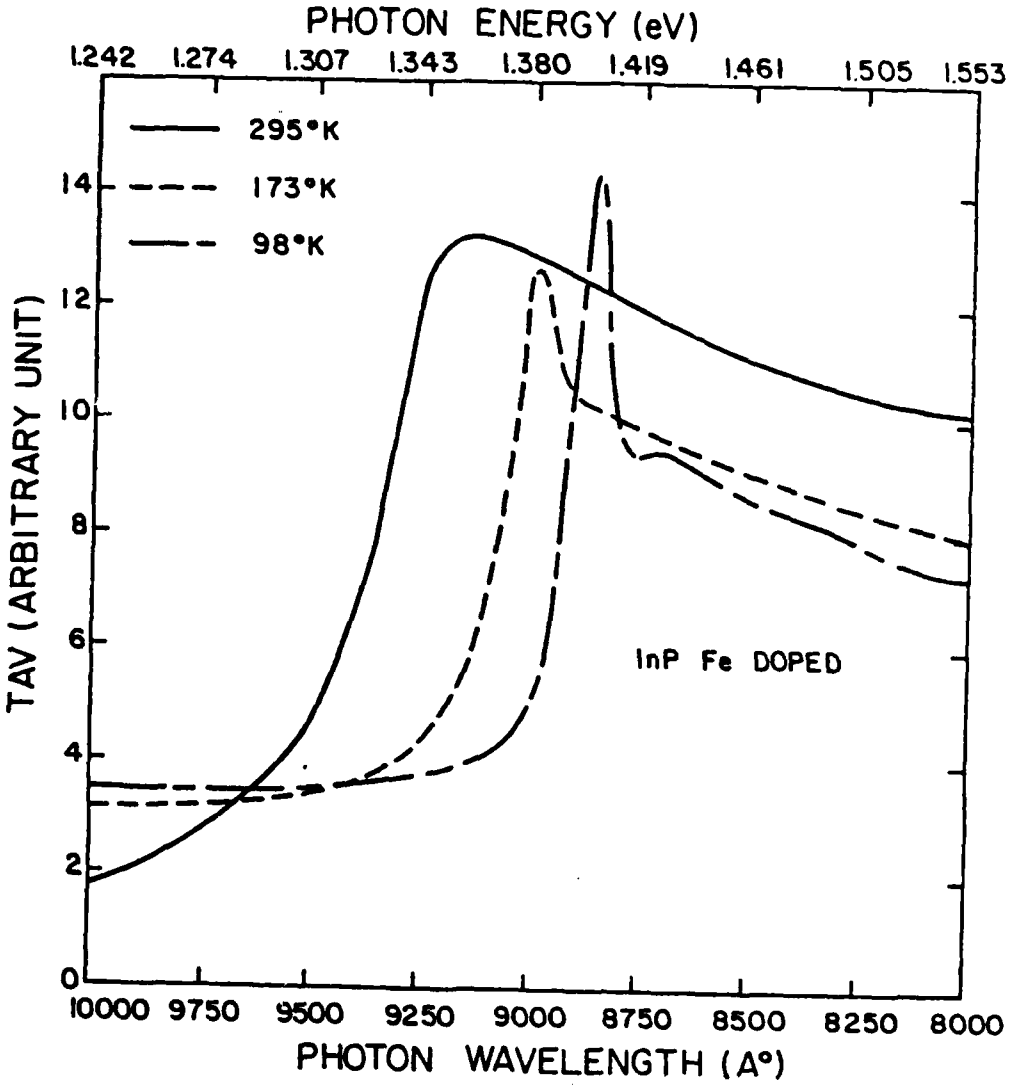


Figure 5.11 One beam TAV spectra of the InP:Fe, exhibiting the exciton peak at lower temperatures.

TAV peak at 1.3 eV is partially due to the electron transfer from E_{D1} donor level to E_{A1} acceptor level which reduces the transition of electrons to the conduction band, and partially due to the increase of the hole density.

The bias light at 900 nm, induces the transition of electrons from E_{D1} level to the conduction band, and thus it increases only the electron concentration. Therefore this bias light has an opposing effect as compared to 1250 nm bias light and it enhances the exciton peak. The TAV amplitude at all wavelengths also increses due to the increase of the electron conductivity. As the bias light photon energy approaches the bandgap, the exciton enhancement effect decreases. At bias photon energies higher than the bandgap (photon energy $\simeq$ 1.52 eV) the exciton peak is even quenched slightly (not shown in figure 5.10) although the overall TAV amplitude is increased. The reason is that in this case both electrons and holes are generated at large numbers, and thus they increase the exciton recombination rate and also screen the Coloumb attraction. The overall TAV amplitude increases because of higher electron mobility.

The persistent quenching effect of the photoconductivity or optical absorption observed at low temperatures [90-92,94] might also be attributed to the presence of the E_{A2} level [85]. At low temperature, by shining the 1 eV light, the electrons get trapped at the E_{A2} level without further transition to the conduction band. Thus the increased hole density causes a high recombination rate and induces the quenching effect. By illuminating the sample with

bandgap radiation, the number of electrons and holes increase equally, not changing the quenching condition appreciably. However, if only the electron concentration increases, without any further increase in the hole concentration, the quenching effect can be terminated. The electron concentration can be increased by the electron transition from the Cr acceptor level [91] to the conduction band, by forward biasing the sample [94] or by increasing the temperature [90,91,94] (which releases the electrons from the E_{A2} level).

In this section the exciton and sub-bandgap absorption is studied by TAV spectroscopy at low temperature. The effects of different bias wavelengths in the quenching and enhancement of exciton peak is discussed. The results indicate the carrier transition to and from acceptor and donor levels, centered around 0.4 eV and 1.3 eV below the conduction band, respectively. These levels can be due to the intrinsic nature of the GaAs surface and associated with Ga and As empty and filled states respectively. The interface state model obtained in this section, confirm and complete the analysis of the previous section. The possible explanation of the persistent photoconductivity quenching effect is discussed based on this model.

5.3 The Effects of Oxidation Rate on the Characteristics of Al/Anodic Oxide/GaAs MOS Structures [83,84]

In the previous section it was shown that the anodic oxidation of high resistivity GaAs increases the interface states density and higher oxidation current density produces a larger interface

states density. In this section the analysis is extended to low resistivity GaAs, and the effects of oxidation rate on the interfacial region and oxide bulk properties are studied. The oxidation rate is controlled by adjusting the oxidation current density. The anodic oxidation mechanism and GaAs/oxide interfacial characteristics are discussed in section 5.1.4. A brief summary is presented here.

The electrical properties of the GaAs/anodic oxide, MOS structure are strongly affected by a large density interface state band (ISB) [78,79]. The anomalously high density of these states gives rise to a complicated C-V characteristic such as the strong frequency dispersion in the accumulation region for n type samples, high total inversion capacitance for p type samples and the field induced hysteresis effect. The density of interface states is affected by initial phase of oxidation which determines the structure and chemical composition of the GaAs/oxide interfacial region [47,83,84]. The bulk properties of the oxide such as the breakdown field and the resistivity should be dependent on the As_2O_3/Ga_2O_3 ratio in the oxide bulk [83,84] (higher ratio results in a superior oxide bulk quality).

In this section the AGW electrolyte (section 5.1.1) is used for the anodic oxidation of n and p GaAs samples at room temperature. The oxide growth rate is controlled during the following two oxidation phases (section 5.1.4). Phase (a) nucleation and island growth, phase (b) coalescence of islands and continuous

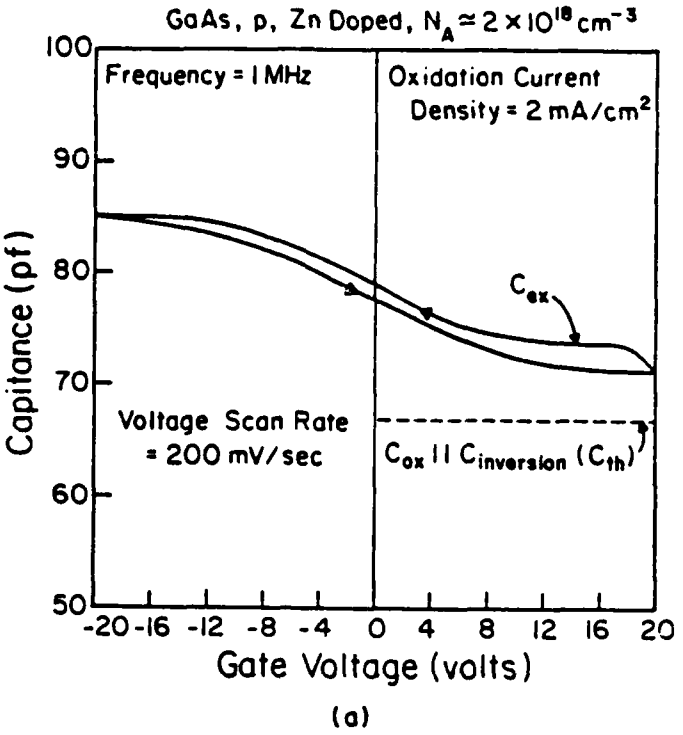
oxide growth. During phase (a) the GaAs/oxide interfacial region forms with the nucleation of Ga_2O_3 at the GaAs surface [140]. Low oxidation rate is desirable in this phase in order to obtain an amorphous and uniform interfacial region with smaller defect density (section 5.1.4). In phase (b), during which the bulk of the oxide is formed, the concentration of the arsenic oxide which is formed and becomes a part of the oxide layer increases, if the oxidation rate is faster, thus producing a higher As_2O_3/Ga_2O_3 ratio. The GaAs/oxide properties are studied under different oxidation schemes as follows.

5.3.1 Oxidation Under Constant Current Densities in Both Phases (a) and (b)

The n and p, GaAs samples are oxidized at different oxidation current densities (J_{ox}). For each oxidation process J_{ox} is constant during phases (a) and (b). Polished samples with the following parameters are used. GaAs, p type, Zn doped, $N_A \simeq 2 \times 10^{18}$ cm^3, $\rho \simeq 0.013\ \Omega cm$, (111) B. GaAs, n type, Te doped, $N_D \simeq 8 \times 10^{16}$ cm^{-3}, (100). The oxidation current densities are 0.2, 1, 2 mA/cm^2. The lower limit of the oxidation current density is determined by the oxide dissolution rate in the electrolyte and it is about 0.01 mA/cm^2 for AGW electrolyte. The upper limit of the current density is effectively determined by the voltage drop across the electrolyte, the GaAs and the external circuit in the initial oxidation phase, and it is about 15 mA/cm^2. The oxidation cell consists of GaAs/AGW electrolyte/pt. The n-GaAs samples are illuminated by collimated

white light during the oxidation. The oxide thicknesses are about 1100 ± 100 A^{o}. The MOS structures are fabricated by evaporating Aℓ dots (15 mils diameter) as the gate electrode. The samples are annealed at 280° C in nitrogen for about one hour. The cell voltage versus time curves are similar to figure 5.1 with different nucleation time and slope (in the linear region) at different oxidation current densities.

The C-V measurements at different frequencies are performed (100 Hz to 1 MHz) and typical C-V plots for p and n samples are shown in figure 5.12. The anomalies that are observed in C-V plots are as follows: a) The inversion capacitances, obtained for p type samples are larger than the calculated values. It should be noted that in calculating the inversion capacitance the errors due to uncertainties in doping concentration and oxide thickness exist. In spite of that the measured inversion capacitance (C_{ex}) is always larger than the theoretical value (C_{th}) (figure 5.12a). n type samples do not exhibit this effect. b) For n type samples a strong frequency dispersion in the accumulation region is observed (figure 5.12b). The accumulation capacitance at higher frequencies (> 10 KHz) is considerably smaller than low frequency values. This effect is much weaker for p type samples. c) A field induced hysteresis can be observed in both n and p C-V plots at room temperature (noted by ΔV in the solid line curve in figure 5.12b). There is also a decrease of the measured capacitance in the scan direction from zero bias voltage towards inversion, as shown in the



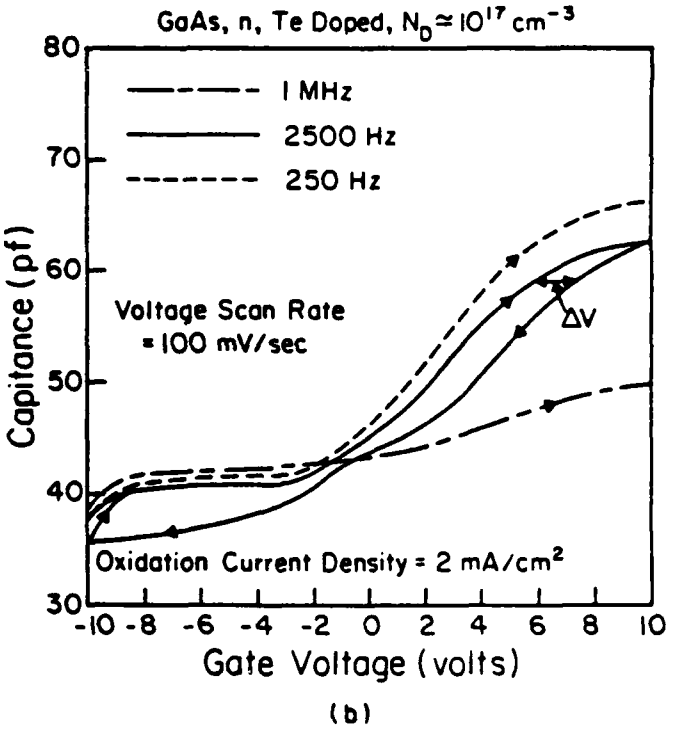


Figure 5.12 Typical experimental C-V plots obtained for the GaAs MOS structures for p, n type samples.

solid curve for n type sample (figure 5.12b). This effect is not an anomaly and is due to the long minority carrier generation time (long compared to the voltage scan rate) in the deep depletion region. This effect can be used to determine the generation lifetime [67,68]. To characterize the oxide bulk properties, the I-V and C-V curves of the MOS structures are used in order to estimate the oxide resistivity and breakdown field. The oxide resistivities are above 10^{14} Ωcm for all the samples. The frequency dispersion of the accumulation capacitance for n type samples, oxidized at different J_{ox} are shown in figure 5.13. In this figure the ratio of the accumulation capacitance (C_{acc}) to the low frequency capacitance ($C_{\ell f}$) is plotted against the measurement frequency, at a fixed accumulation bias voltage. This figure shows more or less the same frequency dispersion behavior for all the samples. The deviations of the experimentally measured inversion capacitance from the theoretical values for p type samples ($C_{ex} - C_{th}$) are shown in Table 5.1, along with the oxide breakdown fields for both n and p samples. The samples which are oxidized, using smaller oxidation current density, exhibit a smaller ($C_{ex} - C_{th}$) as well as smaller breakdown fields. The above phenomena can be discussed as follows.

The basic, single time constant equivalent circuit of the MOS structure which includes the effect of interface states is shown in figure 5.14a (depletion condition). In this figure C_{ox} is the oxide capacitance, C_d is the semiconductor depletion region capacitance, and C_s, R_s are the capacitance and resistance associated

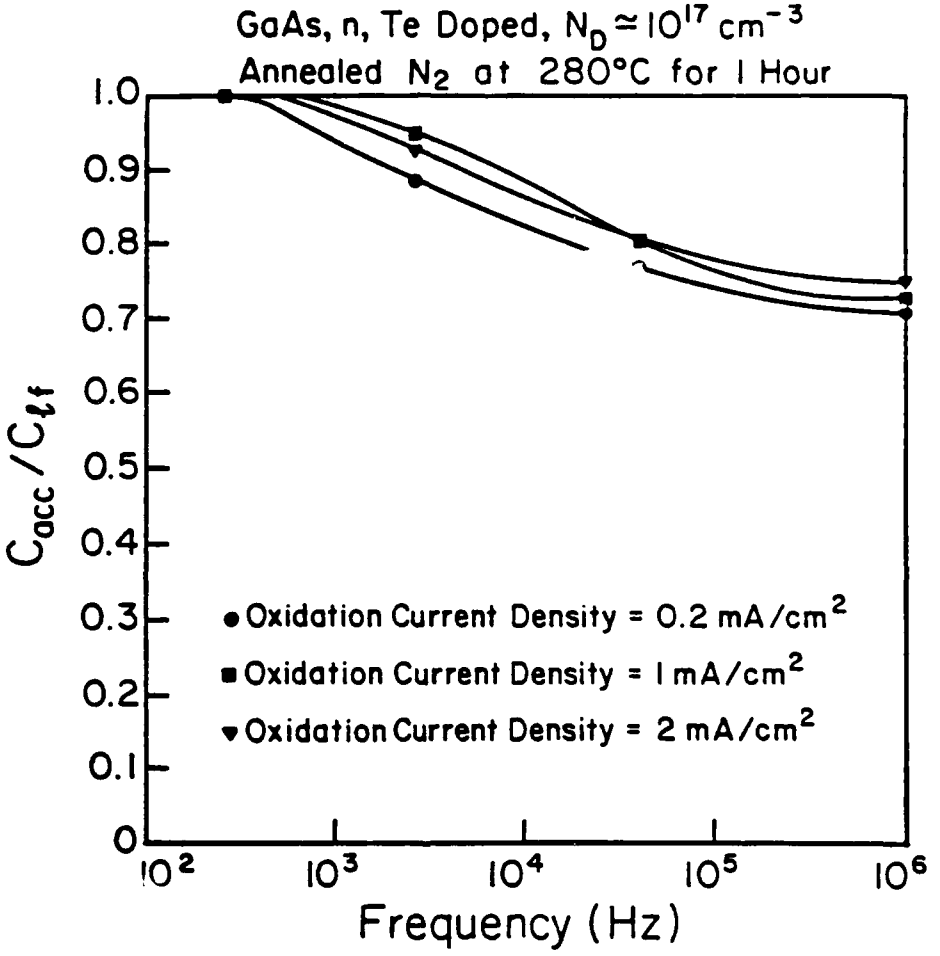


Figure 5.13 Frequency dispersion of the accumulation capacitance for n type GaAs samples oxidized at different oxidation current densities.

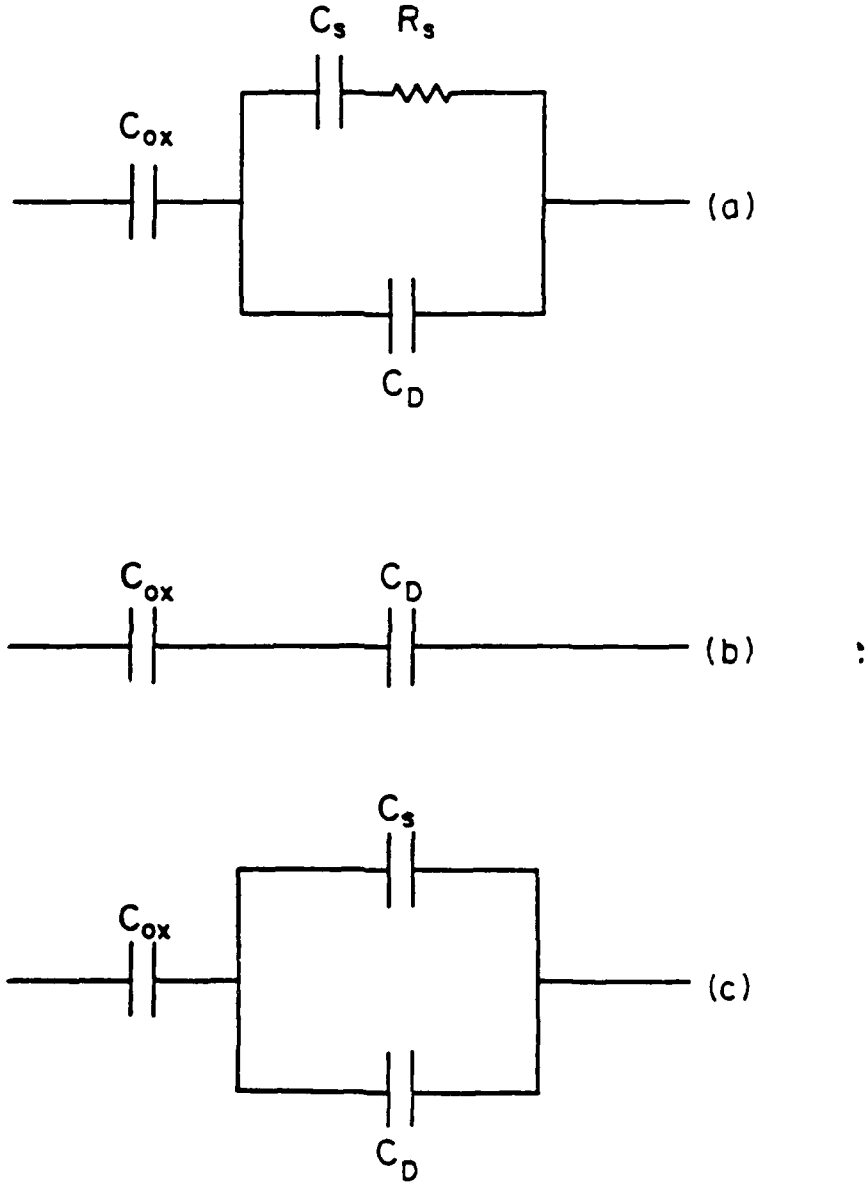


Figure 5.14 Equivalent circuit of the MOS structure under depletion, which includes the effect of the interface trap level (single time constant). a) intermediate frequency, b) high frequency, c) low frequency.

Oxidation Current Density mA/cm^2	GaAs, p $C_{ex} - C_{th}$ (pf)	GaAs, p Breakdown Field V/cm	GaAs, n Breakdown Field V/cm
0.2	5.4	1.8×10^6	2×10^6
1	6.8	2.0×10^6	2.2×10^6
2	7.3	2.4×10^6	2.6×10^6

GaAs, p, Zn doped, $N_A \simeq 2 \times 10^{18}$ cm^{-3}

GaAs, n, Te doped, $N_D \simeq 1 \times 10^{17}$ cm^{-3}

Table 5.1

The effect of the oxidation current density on the properties of GaAs/anodic oxide MOS structure (constant current density)

with interface states which are functions of the surface potential [58]. At high measurement frequencies the interface traps fail to respond to the ac perturbation and the equivalent circuit shown in figure 5.14b results. It should be noted that the interface states still respond to the slowly varying bias voltage and thus they affect the modulation of the surface potential (stretch out effect, discussed in Chapter 3). If the density of interface states is very high at some portion of the bandgap, then in that region the surface potential cannot be modulated by the bias voltage. The reason is that the charges needed to support the bias electric field can be readily supplied by the interface states, instead of the semiconductor depletion region (figure 3.8). In this case the depletion capacitance (C_d) deviates considerably from the ideal value (no interface states). This situation is present in the accumulation region of the n type GaAs. As will be seen shortly the surface of the GaAs cannot be accumulated due to the presence of a high density acceptor band in the upper half of the bandgap. At low frequencies the interface states respond readily to the ac perturbation signal and this results in the equivalent circuit shown in figure 5.14c. The reason that a higher capacitance can be measured in the accumulation region of the n-GaAs at lower frequency (figure 5.12b), is the contribution of C_S (in parallel with C_d) which has a large value (as compared to C_d). In this case the total measured capacitance can approach the oxide capacitance, even though the surface has not been accumulated (C_d is small). By using the single time

constant model which is considered here for qualitative discussion of the effect of interface states, the complex behavior of the C-V and G-V measurements cannot be predicted accurately. Even the statistical model of the interface states which is used successfully to explain the time constant dispersion in G-V measurements of silicon MOS structure [59], does not yield accurate results as compared with the experimental data for GaAs. In this model a set of parallel R_s C_s branches are added to the equivalent circuit shown in figure 5.14a, which account for statistical fluctuations of the surface potential at the interface.

The model which results in the best fit to the experimental C-V and G-V data, considers an exponentially decaying spatial distribution of interfacial traps into the insulator [78,79]. In this model (discussed in section 5.1.4) the interface levels communicate with the GaAs bands by tunneling through the oxides. The time constant dispersion results from the different depths (distance from interface) of the interface levels, and the levels closer to the interface communicate with GaAs very rapidly while the deeper interface levels are slower. The energy distribution of the interface levels is U shaped with anomalously high values in the upper half of the GaAs bandgap. According to this model the interface levels constitute a band above a certain energy level in the upper half of the bandgap, and below a certain energy in the lower half of the bandgap. Within these interface states bands (ISB) the electronic states are non localized and transitions between states are frequent. The high density of

the interface states which are acceptor like at the upper half of the bandgap does not allow the accumulation of the n type GaAs and the full inversion of the p type GaAs. This effect is shown in figure 5.15. In both n and p-GaAs, a high density of acceptor levels in the upper half of the bandgap is shown. For n type samples under accumulating bias voltage the interface states supply the excess negative charges which are needed to support the bias electric field. Therefore the surface potential does not move towards accummulation. This is the reason that the high frequency capacitance is smaller than the oxide capacitance in the accumulation region. The same argument applies for the p type GaAs, except that in this case the surface cannot be inverted (figure 5.15b). Thus it is shown that the modulation of the surface potential is limited to the lower half of the bandgap for both n and p-GaAs which explains the C-V anomalies exhibited in figures 5.12a,b. The presence of the interface states which communicate with GaAs by tunneling through the interfacial region, also explains the field induced hysteresis (oxide charging effect), observed at room temperature. The frequency dispersion effect which is shown in figure 5.13 does not exhibit an appreciable difference for n-GaAs samples oxidized under different current densities. But the data presented in Table 5.1 shows that the $C_{ox} - C_{th}$ (which is related to interface state density) for p-GaAs is smaller for the samples oxidized at lower current density. The breakdown field increases as the oxidation current density goes up, for both p, n GaAs. The higher

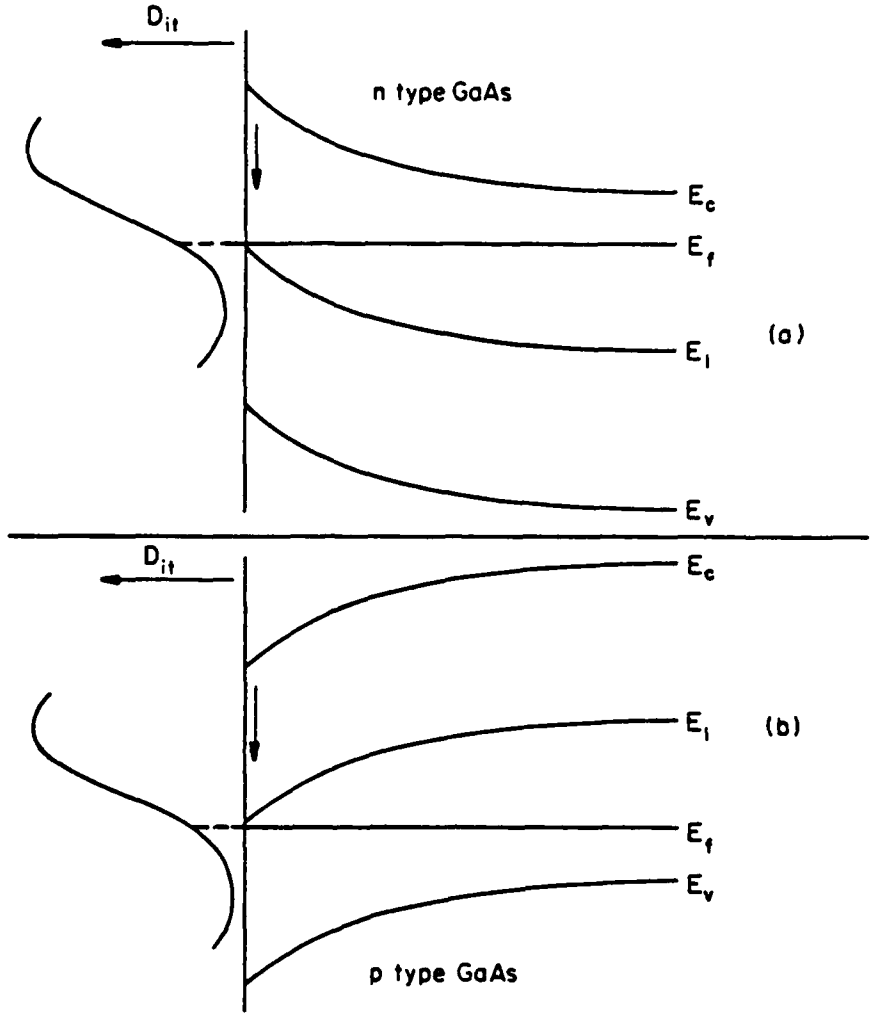


Figure 5.15 The effect of the high density interface states at the upper half of the GaAs bandgap in limiting the modulation range of the surface potential. a) n type GaAs, b) p type GaAs. In both cases the surface potential modulation is limited to the lower half of the bandgap, therefore the n type samples cannot be accumulated, whereas p type samples cannot be inverted.

breakdown field is attributed to the higher As_2O_3/Ga_2O_3 ratio and less incorporation of contaminents and water related traps in the oxide bulk. Therefore overall, it can be concluded that the lower oxidation current density produces a lower density of interface states while the oxide bulk quality is poorer at low oxidation current density. This result is in agreement with the results obtained previously (section 5.1). It seems reasonable that an oxidation scheme which starts with low current density in the nucleation phase and then increases the current density in the continuous oxide growth phase, should yield a lower density of interface states without sacrificing the oxide bulk quality. In the next section, the oxidation schemes using varying current density are investigated.

5.3.2 Oxidation Under Varying Current Densities in phases (a) and (b)

The oxidized samples are n type GaAs, Te doped, $N_d \simeq 8 \times 10^{16}$ cm^{-3}, (100). The oxidation is performed in AGW electrolyte. A voltage controlled current source is used to adjust the oxidation current density. The cell voltage is measured across the GaAs and pt counter electrode (section 5.1.1). The native oxides on the samples are removed by HCℓ prior to the oxidation and samples are illumianted by strong white light during the oxidation.

Three oxidation shemes are used in this study: (1) low current density in phase (a) followed by high current in phase (b),

(J_{ox} = 0.1 → 0.45 mA/cm^2), (2) high current density in phase (a) followed by low current in phase (b), (J_{ox} = 0.45 → 0.2 mA/cm^2), (3) steady current density in phases (a) and (b) (J_{ox} = 0.3 mA/cm^2). The final voltage drop across all of the oxides is about 80 volts. The plots of the cell voltage versus time for different oxidation schemes are shown in figure 5.16. The transition voltage at which the current density is varied is 2.5 volts and 50 volts for oxidation schemes (1) and (2) respectively. Trace (1) shows the slow nucleation phase followed by a rapid growth for scheme (1) (current density: low → high). It is estimated that the nucleation phase is about 350 sec for the 0.1 mA/cm^2 current desnity [47] (section 5.1.1). Therefore this phase should be completed before the current density is switched to 0.45 mA/cm^2 at the 2.5 volts transition voltage. Trace (3) is for the steady state current density with a short nucleation phase. Trace (2) represents the fast initial oxide growth followed by a slower growth rate for the scheme (2) oxidation.

To evaluate the oxide properties the C-V plots are used. The MOS structure is fabricated by Aℓ evaporation on the oxide (diameter = 15 mils) as the field plate and gold is sputtered on the GaAs back surface as the substrate contact. The samples are then annealed at 260° C in nitrogen ambient for about 50 minutes. The oxide thickness after annealing is about 1000 ± 100 A$^{\circ}$, as calculated from the C_{ox} value measured by low frequency C-V in the accumulation region (oxide relative permitivity ≈ 10). The C-V

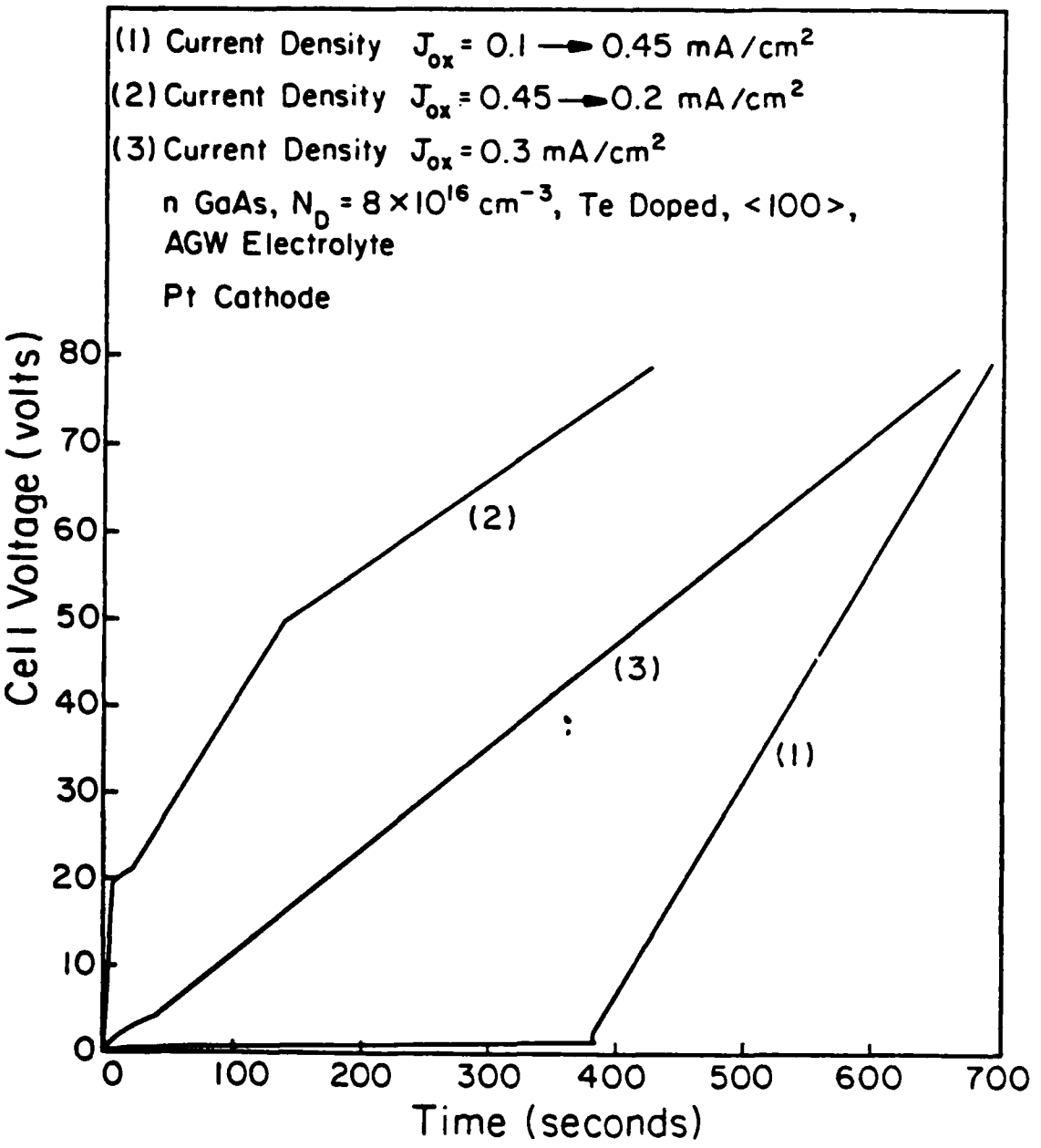


Figure 5.16 Oxidation cell voltage versus time curves for low resistivity, n type GaAs samples, oxidized under different oxidation current density schemes.

measurements are performed in the frequency range of 10 Hz - 1 MHz. The C-V plots of the oxidized GaAs (scheme (1)) at low and high frequencies are shown in figure 5.17. The injection type hysteresis is estimated from the flatband voltage shift (ΔV_{FB}) between the opposite scan directions. The high frequency curve is used for the estimation of the interface states density within the bandgap by the Terman method [113]. In this technique the high frequency C-V curve is compared to the ideal theoretical C-V curve (no interface states). At each value of the capacitnace the gate voltage shift (ΔV) versus the gate voltage can be obtained. The surface state charge is then $Q_{it} = C_{ox} \Delta V$. By evaluating the surface potential (V_s) at each gate voltage, the surface state density is obtained from the slope of the Q_{it} versus V_s. For comparison between different oxidation schemes, the interface states density at around midgap is compared for different samples.

The values representing the field induced hysteresis, the density of interface states and the oxide breakdown fields are summarized in Table 5.2. The oxide resistivity is also measured which is on the order of 10^{15} Ωcm for all the samples. The numbers in Table 5.2 indicate the following: 1) The magnitude of the injection type hysteresis is tne smallest for low → high oxidation. This parameter can be dependent on both the interface and oxide bulk properties. 2) The interface state density, measured at the maximum of the accumulating bias voltage is also the lowest for the low → high scheme, indicating a lower defect density at

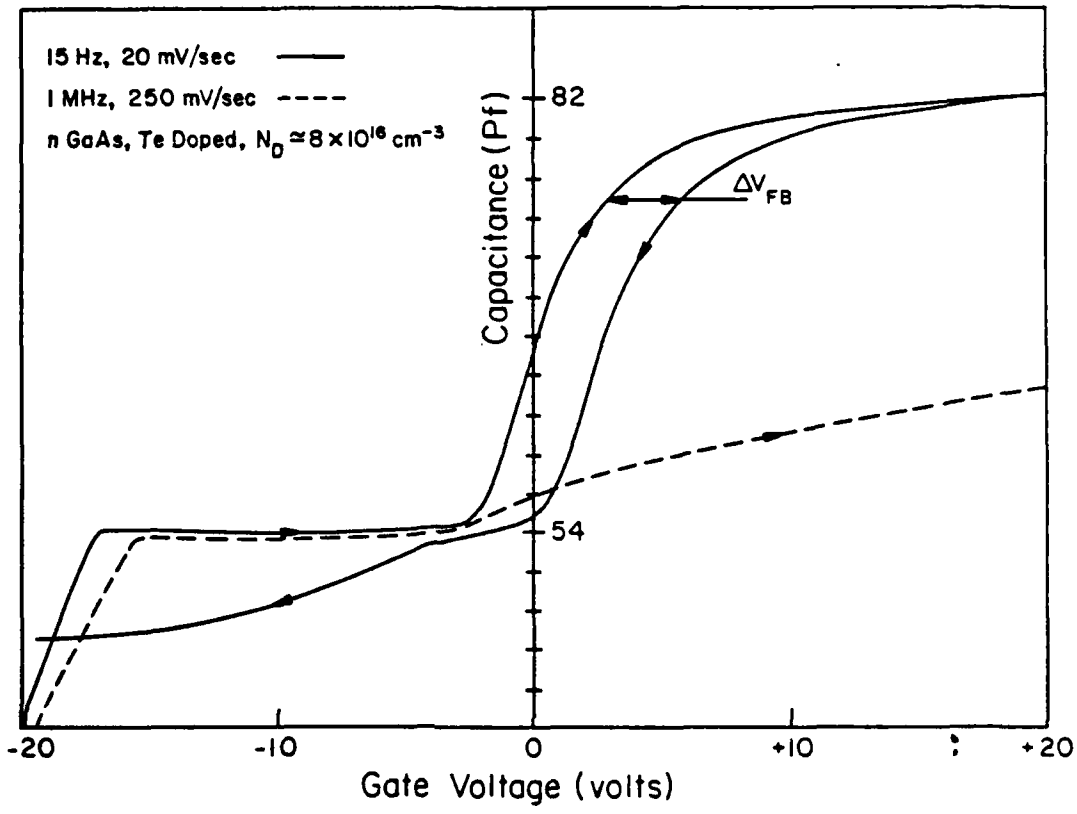


Figure 5.17 Low and high frequency C-V plots of the anodically oxidized n-GaAs using oxidation scheme (1).

Oxidation Scheme	Current Density mA/cm^2	Injection Type Hysteresis/cm^2-V	Interface State Density/cm^2 - eV at Midgap	Breakdown Field V/cm
1) Low → High	0.1 → 0.45 Transition voltage = 2.5 volts	1.8×10^{10}	1.5×10^{13}	5.6×10^{6}
2) High → Low	0.42 → 0.2 Transition voltage = 50 volts	2.3×10^{10}	2×10^{13}	5.8×10^{6}
3) Steady	0.3	3.1×10^{10}	2.4×10^{13}	5.8×10^{6}

Table 5.2

Comparison between the effects of the different oxidation schemes in determining the GaAs/anodic oxide parameters (varying current density)

GaAs/oxide interface. It should be noted that even at this bias voltage the surface potential is around midgap and the surface is not accumulated. The somewhat better characteristic of the high → low over the steady current scheme regarding the above parameters might be due to the fact that, during the initial oxidation phase, the current density is almost the same in these cases. But the higher current density of scheme (2) in most of the oxidation process (transition voltage ≃ 50 volts) can produce a better quality oxide bulk. 3) The breakdown field for all cases is about the same with a value in excess of 5×10^6 V/cm, indicating a good quality of oxide bulk.

The results presented in this section agree with the results and analysis presented in the previous sections [47,83]. It is reasonable to believe that the high density of interface states is an inherent nature of the GaAs/oxide interfacial region and it is not strongly dependent on the carrier type or concentration (the results are more or less the same for n, p or high resistivity GaAs). The two beam TAV spectroscopy is used for the interface study of high resistivity GaAs, and it has the advantage that both oxidized and unoxidized samples can be readily studied. The high sensitivity of the TAV technique at low carrier concentrations is utilized to characterize the samples with a resistivity range ($\rho > 10^7$ Ωcm) at which the C-V measurements are not applicable. The overall results for all the samples (n, p, high and low resistivity) indicate that the oxidation tends to increase the density

of interface states, but by using a lower initial oxidation current density, this effect can be minimized. In general the interface states density is still too high ($\simeq 10^{12}/cm^2$ - eV at its minimum value) for the routine fabrication of the GaAs, MOS based LSI circuits with long term stability. However it is shown that by utilizing the control of the oxidation current density (oxidation rate) during different oxidation phases, the interface and bulk properties can be improved simultaneously and one can reduce the interface states density without lowering the oxide bulk breakdown field.

CHAPTER 6

STUDIES ON CdS, InAs, AND HgCdTe

This chapter includes the following papers:

1) P. Das, R. T. Webster and B. Davari, "Electrical Properties of Semiconductor-Electrolyte (CdS-$NiCl_2$) Using Surface Acoustic Wave Techniques", Appl. Phys. Letters, Vol. 34, pp. 307-309, 1979.

2) F. M. Mohammed Ayub and P. Das, "Spectroscopy of InAs Using SAW Generated Transverse Acousteolectric Voltage", J. Appl. Phys., Vol. 51, pp. 433-436, 1980.

3) P. Das, M. Tabib-Azar, B. Davari and J. H. Everson, "Characterization of Mercury Cadmium Telluride Using Non-Destructive Transverse Acousto-Electric Voltage Measurements", 1983 Ultrasonics Symposium Proceedings, to be published.

It also consists of a part of Mr. Bijan Davari's Master Thesis entitled "Semiconductor Liquid Junction Solar Cell", pp. 58-77.

Electrical properties of semiconductor-electrolyte (CdS-$NiCl_2$) using surface acoustic wave techniques[a)]

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(Received 6 November 1978; accepted for publication 6 December 1978)

Spectroscopy of the cadmium sulphide–nickel chloride interface has been performed by measuring the acoustoelectric voltage induced by a SAW-delay line. Observation of transitions at different radiation wavelengths is attributed to the presence of electronic levels at the interface.

PACS numbers: 72.20. – i, 73.40.Mr, 68.45. – v

Electronic properties of the CdS surface have been of interest since efficient photovoltaic energy conversion was demonstrated using the Cu$_2$S-CdS heterojunction structure.[1,2] Recently, it has been found that semiconductor-electrolyte junction devices can be used as photovoltaic energy converters with moderate efficiency. CdS has also played an important role in these devices.[3–5] Because of the presence of the liquid electrolyte, the conventional means of studying the electronic properties of the semiconductor surface may not be suitable. A contactless technique of determining electrical properties of the semiconductor surface has been developed using surface acoustic waves (SAW) as a probe.[6,7] This technique has been suitably adapted for application to the semiconductor-electrolyte interface. The purpose of this paper is to describe this modification of the SAW technique and present some experimental results performed on CdS-$NiCl_2$ system.

The SAW semiconductor probing technique relies on the interaction of the electric field which accompanies a SAW propagating on a piezoelectric substrate with the charge carriers of a semiconductor placed near the substrate. The SAW is excited by an interdigital transducer (IDT) fabricated directly on the surface of a piezoelectric crystal. These waves propagate in the vicinity of the surface with a velocity slightly lower than the bulk shear wave velocity of the crystal. The mechanical motions are confined to the surface of the crystal decaying exponentially within the crystal away from the surface and are accompanied by a propagating electric field. Though this electric field is also confined near the surface it exists both inside and outside the crystal. The decay constant of the electric field outside the surface is of the order of the SAW wavelength. For the study of a semiconductor surface, the sample is placed in the proximity of a SAW delay line; this decaying electric field interacts with the carriers in the semiconductor.

Inside the semiconductor, the electric field decays within a Debye length of the surface or within an acoustic wavelength, whichever is shorter. The manifestations of the interaction include the generation of the acoustoelectric voltage, attenuation of the SAW, and a change in the SAW phase velocity.[1] Each of these effects is dependent on semiconductor conductivity. By observing the variation of these parameters while the semiconductor conductivity is changed by illumination or by a biasing electric field, electrical characteristics of the semiconductor can be determined.

The experimental setup is shown schematically in Fig. 1(a). The delay line is Y-cut Z-propagating lithium-niobate, with interdigital transducers deposited at each end. A mechanical arrangement allows placement of the semiconductor in the proximity of the delay line with a uniform air gap. Electrical contact is made at the back of the semiconductor by metal deposition or with a metal plate as shown. This metal contact allows monitoring of the transverse component of the acoustoelectric voltage and can also be used to bias the semiconductor surface. Provision is made to illuminate the semiconductor surface with monochromatic radiation of variable intensity and wavelength. The entire structure can be immersed in a Dewar for accurate-control of the temperature.

The modified experimental arrangement shown in Fig. 1(b) was used to study the semiconductor-electrolyte interface. The replacement of the air gap by a liquid perturbs the

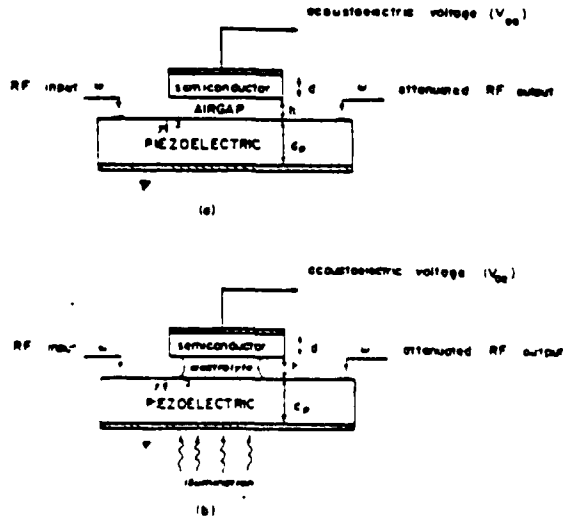

FIG. 1. (a) Experimental set up used in SAW semiconductor investigations. (b) Modified structure incorporating semiconductor-electrolyte interface.

[a)]Partially supported by ONR contract No. N00014-75-C-07720

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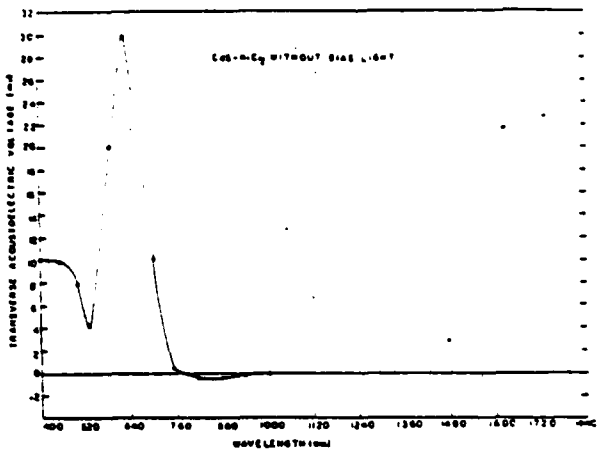

FIG. 2. TAV spectral response for Cds-$NiCl_2$.

surface wave propagation in two distinct ways. First, the attenuation of the surface wave is increased due to the loading of the delay line surface. Second, new waves, such as layer waves, are generated in the liquid, causing additional interaction, particularly if the semiconductor is also piezoelectric as in the case of CdS. Both of these effects have been extensively studied in the CdS-water-$LiNbO_3$ structure in connection with the amplification of SAW's and in parametric signal processing devices.[9,10] The introduction of the electrolyte between the delay line and semiconductor also reduces the sensitivity of the metal plate to detect the transverse acoustoelectric voltage. Much greater sensitivity was obtained when a contact was made directly on the semiconductor surface.

For the study of the CdS-$NiCl_2$ system the acoustoelectric voltage was measured as a function of incident photon energy. The dimensions of the CdS sample were $4 \times 8 \times 2$mm. The interactive surface was flat and polished. A $1M$ solution of $NiCl_2$ was introduced between the delay line and the CdS: 110-MHz surface acoustic wave pulses 300 μsec in duration were used to probe the interface at a 100-Hz repetition frequency. The interface was illuminated with the output of a Baush and Lomb monochromator with appropriate filters to eliminate higher orders. The spectroscopy was also carried out in the presence of a bias light obtained from a mercury arc lamp.

The dependence of the transverse acoustoelectric voltage (TAV) on semiconductor conductivity can be qualitatively described as follows: The electric field associated with the SAW penetrates the semiconductor and modulates the carrier density near the semiconductor surface. This causes a net charge separation, the dc component of which gives rise to the acoustoelectric voltage. When the carrier density and, hence, the conductivity is low, it is obvious that the acoustoelectric voltage will be small. On the other hand, when the conductivity is large, the electric field will effectively be screened by carriers at the semiconductor surface. In this case, the acoustoelectric voltage is once again small. For some intermediate conductivity the electric field fully modulates the charge density and the acoustoelectric voltage reaches a maximum. In addition, the sign of the transverse acoustoelectric voltage depends on the carrier type. That is, 21
n-type semiconductors exhibit a positive TAV, and p-type semiconductors exhibit a negative TAV.

Referring now to the TAV spectral response shown in Fig. 2, the most notable feature is the minimum at 530 nm followed by a maximum at 615 nm. The minimum corresponds to the very high conductivity caused by band-to-band transitions. The fact that the TAV is positive indicates that the conduction is mainly by electrons. As longer wavelengths are used to illuminate the semiconductor, the conductivity decreases since fewer electrons make the transition from the valence to the conduction band. The TAV therefore, reaches a maximum and then decreases in the interval from 760 to 940 nm. The TAV is negative, indicating that conduction is mainly by holes. This suggests the presence of a band of electron acceptors at 1.3–1.6 eV above the valence band. Photons having energies in this range cause transitions of electrons from the valence band to the acceptor levels, leaving free holes behind. For wavelengths greater than 1000 nm, the TAV was too small to detect. Thus, the conductivity in this region is very low.

Figure 3 shows the TAV spectral response when the interface is also illuminated by bias light from a mercury arc source. The horizontal line represents the value of the TAV for illumination by the bias light only. For short wavelengths the shape of the curve is similar to that of Fig. 2. That is, the high conductivity associated with band-to-band transitions causes a minimum in TAV near 530 nm. As conductivity falls, the TAV goes through a maximum. At 760 nm the TAV drops sharply below the value obtained for bias light alone and remains at a low level until 1000 nm. This quenching of the TAV may be explained as follows: A band of electron acceptor levels is present between the energies 1.3 and 1.6 eV, as discussed with regard to Fig. 2. When the bias light strikes the sample, electrons which occupied these states under dark conditions are excited to the conduction band. Now, when photons of appropriate energy excite electrons from the valence band to the acceptor band, a new steady-

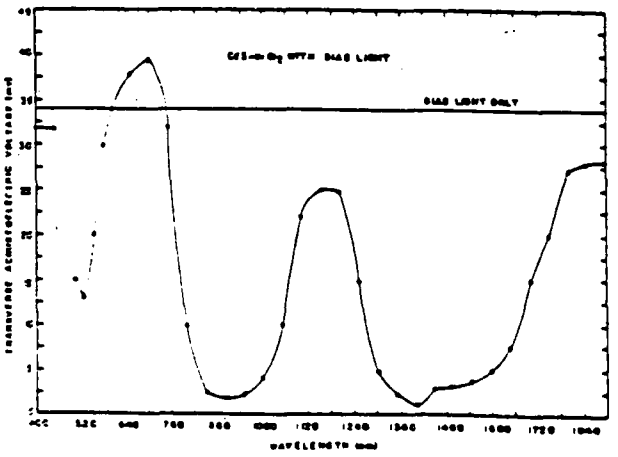

FIG. 3. TAV spectral response for CdS-$NiCl_2$ with bias light from a mercury arc source.

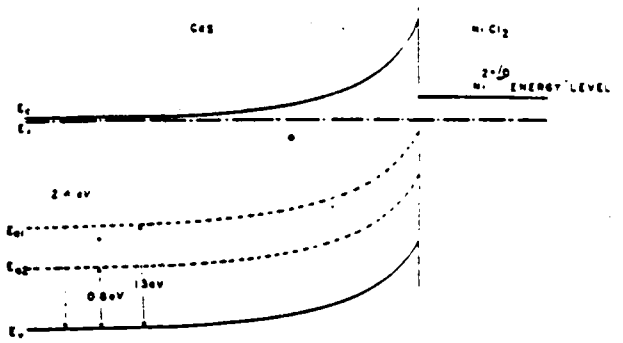

FIG. 4. Energy-band diagram for CdS-$NiCl_2$ system.

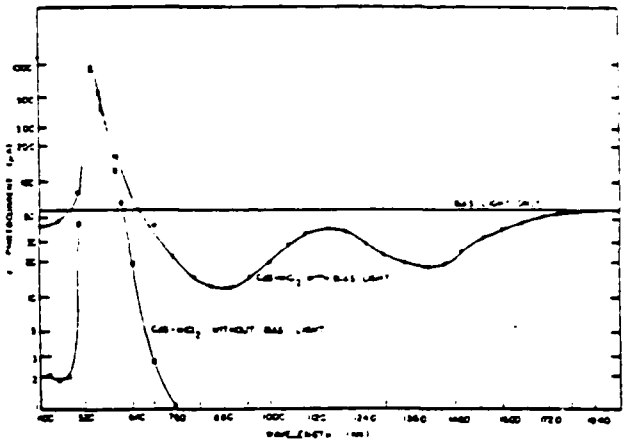

FIG. 5. Photocurrent as a function of illuminating wavelength for CdS-$NiCl_2$.

state condition is obtained in which the concentration of free electrons is lower. That is, the quasi-Fermi level for electrons is drawn downward toward the acceptor level.

For wavelengths greater than 1000 nm, the TAV begins to climb back toward its bias-only value, reaching a maximum near 1180 nm. At this point a second quenching occurs. This effect may be attributed to a second band of acceptors extending from 0.7 to 1.0 eV corresponding to wavelengths of 1180–1780 nm. After this band the TAV returns toward its bias-only value. The band diagram of Fig. 4 illustrates the positions of the acceptor levels. Similar results have been obtained by other researchers.[11,12]

In order to verify that the TAV was indicating changes in the photoconductivity, a measurement of the spectral response of the surface photocurrent was made. The results are shown in Fig. 5, where it can be seen that the conductivity does vary with wavelength in the expected manner. In the no-bias case the photocurrent increases to a maximum at 530 nm, then decreases to a very low value for wavelengths greater than 760 nm. The spectrum with bias shows the same peak at 530 nm and a similar broad minimum from 760 to 940 nm and from 1180 to 1780 nm.

In conclusion, it has been demonstrated that the SAW semiconductor technique can be suitably adapted to detect electronic levels at the interface of a semiconductor and an electrolyte.

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CHARACTERIZATION OF MERCURY CADMIUM TELLURIDE USING NONDESTRUCTIVE TRANSVERSE ACOUSTOELECTRIC VOLTAGE MEASUREMENTS

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Abstract

Hg_{1-x} Cd_x Te is extensively used today as a versatile infrared detector material with increasing importance in the fabrication of focal plane arrays. In this work Hg_{1-x} Cd_x Te electronic properties are investigated using nondestructive SAW technique. The transverse acoustoelectric voltage (TAV) is monitored across the Hg_{1-x} Cd_x Te sample which is placed in proximity of a $LiNbO_3$ delay line. TAV is developed due to the nonlinear interaction between the electric field accompanying SAW, and the free carriers near the Hg_{1-x} Cd_x Te surface. Contactless TAV and surface photovoltage spectroscopy are performed to determine the bandgap and thus the alloy composition (x) of Hg_{1-x} Cd_x Te.

The TAV versus voltage measurements are also performed for further investigation of Hg_{1-x} Cd_x Te surface properties (such as conductivity type and possible surface inversion due to passivation by ZnS).

Introduction

Full scale production for current and future generation military infrared systems will require linear arrays and mosaic focal planes with a large number of infrared detectors. Mercury cadmium telluride provides a predominant role as the material for these detectors.[1] To maintain high volume photo-detector production and maximum yield for systems such as Advanced FLIR Technology (AFT), Thermal Weapon Sights (TWS) and the Shuttle Infrared Telescope Facility (SIRTF), advanced nondestructive contactless techniques will be needed.

For example, a fast, reliable contactless technique is highly desirable for characterizing semiconductor materials at several key production points before completion of the final photodetector. These points may include annealing, slicing, polishing, etching, surface passivation and implant profiling. Contactless testing provides considerable savings in labor and materials by rejecting a faulty device early during production and by making this determination with relative ease compared with other techniques requiring ohmic contacts or metallization. The contactless technique chosen for this paper uses Surface Acoustic Wave (SAW). Different implementations of the SAW technique[2-10] have been used for semiconductors such as Silicon, Cadmium-Sulphide, Indium Arsenide, Indium Phosphide, Gallium Arsenide and Gallium Phosphide. In this paper, it is extended to include Cadmium Telluride (CdTe) and Mercury Cadmium Telluride with varying alloy composition (Hg_{1-x} Cd_x Te).

The main feature of the SAW technique is that the probing tool is an AC electric field which is generated at the surface of a piezoelectric material and is coupled to the semiconductor surface without any form of contact. To produce this electric field the SAW is generated by applying rf voltage to the interdigital transducers made on the surface of a piezoelectric material ($LiNbO_3$)[2,3] as shown in figure 1a. Because $LiNbO_3$ is piezoelectric, the elastic wave is accompanied by an electric field with a component perpendicular to the surface of the $LiNbO_3$ substrate (probing field). This component exists outside the $LiNbO_3$ to a distance of about an acoustic wavelength (≈ 31.6 μm for 110 MHz rf pulse). When the probing electric field reaches under the semiconductor surface (which is placed above the delay line (fig. 1b), the acousto-electric interaction with the free carriers of the semiconductors manifests itself as attenuation and change in velocity of SAW and the appearance of a d.c. voltage across the semiconductor. The transverse component of this voltage which is called the transverse acoustoelectric voltage (TAV) is the monitored signal throughout the following experiments. The penetration depth of the probing field is on the order of the semiconductor extrinsic Debye length or the acoustic wave length, whichever is shorter. TAV signal can be monitored by placing a metal plate above the semiconductor and another one either below the $LiNbO_3$ substrate (fig. 1b) or above it (fig. 1d). To monitor the dc TAV signal through the possible insulators, the rf voltage and thus the probing electric field are pulsed. TAV is capacitively coupled to the metal plates, so the presence or absence of insulator layer on the semiconductor surface is immaterial. The nature of these contacts through which the TAV is monitored is important for a nondestructive measurement. In spectroscopy measurements, the configuration of fig. 1b is used where the ground path is an Al plate evaporated underneath the $LiNbO_3$ and the monochromatic incident beams are shone on the semiconductor surface through a small window. This structure is sufficient for spectroscopic measurements where the modulation of the surface potential by an external dc bias is not needed. On the contrary, if the surface potential has to be modulated, a very large voltage in excess of 1000 volts is needed to sustain the voltage drop across the thick $LiNbO_3$ substrate (≈ 3 mm).[5] To overcome this problem, the new configuration which is shown in fig. 1c is

devised. In this configuration, a thin aluminum structure (≈ 1000 A°) is evaporated on the $LiNbO_3$ surface which provides the ground path for the TAV signal. At the center of the aluminum structure, a window is made which acts as the interaction region. Under the Al covered area the electric field tends to zero while the mechanical wave continues to propagate. Once the mechanical wave reaches the interaction window, the probing electric field is regenerated. The semiconductor under test is placed above the interaction region where the probing electric field penetrates inside the semiconductor and produces the TAV signal (fig. 1d). To change the surface potential a dc voltage is applied across the semiconductor through the same structure used to detect the TAV signal. To complete the circuit an Al plate is pressed on the semiconductor back surface and the ground path is the Al structure on the surface of $LiNbO_3$. The contact to the surface under study (device side) is of special importance. This contact is simply provided by placing the semiconductor on the Al coated $LiNbO_3$ (fig. 1d) and there is no processing involved. The ground path on the surface of the $LiNbO_3$ has reduced the necessary magnitude of the applied dc voltage by a factor of 100 as compared to the previous work[8] due to the elimination of the voltage drop across the $LiNbO_3$.

In this paper the feasibility of the TAV measurement technique to CdTe and $Hg_{1-x}Cd_xTe$ is demonstrated using both the spectroscopy and TAV vs applied bias voltage measurements.

Transverse Acousto-Electric Voltage and Experimental Procedure

TAV measurements in general, consist of monitoring the TAV amplitude or transient time constants while the semiconductor surface condition is varied by an external excitation such as photons, applied bias field and heating or cooling. TAV amplitude dependence on the electronic properties of the semiconductor surface is described elsewhere[10] and is proportional to the conductivity difference between the electrons and holes.

Fig. 2 shows the plot of TAV vs electron and hole concentration using eqn. (15) of reference 10. The constants used for the figure are shown in Table I and the frequency of SAW assumed is 100 MHz. The form of the curve is similar for other semiconductors. The important features of the plot are: 1) n type surface conductivity exhibits a positive TAV and vice versa for p type. 2) There is a maximum in both the n and p regions. The reason is that for the intrinsic case there are few carriers to interact with the probing electric field and the TAV is very small. As the concentration of the free carriers increases, the TAV grows until it reaches the maximum. At higher conductivities, the free carriers begin to screen the probing electric and the TAV amplitude reduces. Thus by monitoring the TAV amplitude one can distinguish between electron and hole surface conductivities and also obtain the magnitude of the surface conductivity. Because of the large difference in electron and hole mobilities, the peak TAV of n-type samples is much larger than that of p-type. Because of the large bandgap of CdTe, TAV is predominantly in small regions of electron and hole concentrations. One should note the high sensitivity of the TAV signal at very low carrier concentrations which extends the measurement capability to very high resistivity samples. This is a distinct advantage over other measurement techniques such as Hall voltage and four point probe measurements. On the other hand, the sensitivity of the TAV technique decreases at very high carrier concentration. Lock-in detection of the TAV amplitude has alleviated this problem to some extent.

In the experiments reported here, the rf pulse applied to the input transducer has frequency of 110 MHz (55 MHz is also used) and its amplitude is about 10 volts P/P (50 Ω load resistance). The pulse duration is in the range of μ sec. with repetition rate of about 30 Hz. The TAV amplitude is measured by a lock-in amplifier locked to the envelope of the rf excitation pulse. In some cases the TAV amplitude is recorded manually.

Fig. 3 shows a typical input and output of the SAW delay line and the resulting TAV when HgCdTe is used. In this picture trace (a) is the 110 MHz input rf pulse with about 2.5 μsec. Trace (c) shows the TAV signal obtained from the HgCdTe sample which is about 7 μsec delayed with respect to the input rf pulse. The first peak in trace (c) with no delay (the small peak) is due to the radiation from rf input pulse.

The time constant associated with the leading edge of the TAV signal can be related to the generation lifetime (τ_g) and surface generation velocity (S_g).[6] The separation of τ_g and S_g is possible by the application of a depleting dc bias field across the semiconductor.[7] τ_g and S_g are determined for silicon wafers (used for VLSI fabrication) as an indication of the defect density. These parameters can be depth profiled by the new technique introduced in reference 5. However, these experiments have not been performed as yet for CdTe or HgCdTe samples.

Spectroscopy of TAV amplitude is used to reveal the subbandgap absorption and the interface states energy band structure of the semiconductors. In this method, the wavelength of the incident beam is scanned in the desired range. The detection sensitivity of the subbandgap structures can be enhanced by two beam spectroscopy as compared to one beam, by the proper choice of the bias light wavelength.

The monochromatic incident incident beam is chopped with a mechanical chopper which also provides the reference signal for the lock-in amplifier and the pulse generator. Bausch & Lomb monochromator (B & L Cat. #33-86-25 with high intensity tungsten source) is used for the wavelengths in the range of 500 to 3000 nm. The TAV amplitude is recorded and plotted against the wavelength. To obtain the desired wavelength range, three gratings are used covering (500-750 nm), (700-1150 nm) and (1150-3000 nm) ranges. The incident photon flux is kept constant up to 2100 nm (by experimental

calibration using a thermopile) and its 7×10^{14}/cm^2 sec. For the wavelengths higher than 2200 nm the monochromator output is not experimentally calibrated and only the spectral flux output curve, furnished by the manufacturer, is used (for grating 33-86-04). This spectral flux exhibits a strong decrease of the output power for wavelengths beyond 2750 nm. A high resolution HRS-1 (Jobin Yvon) monochromator with 300 grooves/mm grating is also used in the spectral range from 1600 to 3200 nm. The resolution of these measurements is about 125 A° (lowest resolution is used to obtain a higher output flux).

TAV measurements under the applied dc bias (which modulates the surface potential and the depletion width) are of great importance. Both TAV amplitude and transient time constant dependence on the bias voltage (TAV-V and τ-V) are utilized. In these experiments the new delay line structure (fig. 1c,d) is used. TAV-V plots can be used as a nondestructive alternative to C-V measurements in order to determine the oxide charge and flat band voltage of thermally oxidized silicon wafers.[2] A new profiling technique is devised which is applicable to the measurements which are primarily sensitive to the free carrier concentration rather than the depletion layer thickness.[5] By using this technique and the TAV-V plots, the free carrier concentration depth profile can be obtained[5] similar to the differential capacitance methods. In the TAV-V experiments, the first harmonic of the TAV signal which is directly proportional to the TAV amplitude is monitored by a lock-in amplifier. The external bias voltage is scanned over the desired range (typical range = ±10 volts) and the TAV-V is recorded. The operation is simple and there is no need to fabricate any form of contact (e.g., MOS, pn, or Schottky barrier) to the semiconductor surface. The time constants associated with the TAV transients are monitored under the applied bias voltage[7] in order to determine the generation lifetime (τ_g) and surface generation velocity (S_g). Using the TAV-V and τ-V plots simultaneously, the position of the recombination center within the semiconductor bandgap can be determined.[7]

Results and Discussion

The properties of the samples used for different experiments are listed in Table II. Sample A is $Hg_{1-x}Cd_xTe$ with $x = 0.4$. No special surface passivation was performed for this sample. Sample B has a 3500° A thick zinc sulphide passivation layer. Sample C is CdTe and is included in the study as CdTe is often used as the substrate material for growing HgCdTe by liquid phase epitaxy.

TAV Spectroscopy

TAV and photo-voltage spectra for Sample A are similar and shown in figure 4. The spectrum is used to estimate the bandgap and thus the alloy composition (x) of the HgCdTe sample. Figure 3 shows that for wavelengths higher than 2000 nm there is a strong minimum around 2350 nm and also the response falls off sharply for wavelengths higher than 2500 nm. Minimum around 2350 nm is partially attributed to the monochromator spectral flux and partly to the sample's optical characteristic. The wavelength corresponding to the half peak value of the spectral response (the cut off wavelength, λ_{co}) is about 2500 nm or 2.5 μm. Thus the bandgap can be estimated to be about:

$$E_g = \frac{1.24}{2.5} = 0.5 \text{ eV}.$$

The corresponding alloy composition (x) is estimated by linear interpolation of the data presented in ref. 1 and it is about 0.44 which is in reasonable agreement with the value obtained by density measurements. The presence of discrete defect levels at HgCdTe surface influences the spectra and might explain the rest of the structures. However, to pinpoint their effect, one needs to perform the two beam spectroscopy which has not yet been performed.

TAV-V Measurement

In Figs. 5, 6, and 7 the TAV-V plots are given for Samples A, B and C respectively. TAV polarity is negative at zero bias voltage (sample A) indicating a p type surface conductivity. In HgCdTe semiconductor the electron mobility is about 100 times higher than the hole mobility. Since the TAV signal is related to the conductivity difference between electron and holes, it is possible to obtain positive TAV polarity even if the electron concentration is about 100 times less than hole concentration. By applying a positive D.C. voltage to the HgCdTe surface, the electron conductivity increases (due to the increase in the surface electron concentration) and the negative TAV amplitude decreases. For further increase in voltage, the surface conductivity changes from p to n type, and at around .15V the TAV is zero and then the TAV polarity is reversed to positive sign (indication of n type surface conductivity). It should be noted that in fig. 5 the horizontal coordinate is the value of the applied D.C. voltage across the HgCdTe (fig. 1(c)). In the negative direction, the holes increase due to accumulation. TAV initially increases in the negative direction, reaches a peak at -0.1V and by further increase of the voltage in the negative direction, it decreases due to the screening affect of the holes. Curves similar to fig. 5 have been obtained for many samples. In all the figures, the shape of the curve remains more or less the same although the voltage axis is shifted indicating a different flatband potential and possible different contaminant charges on the semiconductor surface. C-V measurements on similar samples also show this change in the surface charge density for unpassivated surfaces.

Fig. 6 shows the TAV-V for ZnS passivated HgCdTe sample. Comparing figs. 5 and 6 we note that there is a shift of (-0.8 -(-0.15)) = .95V in the applied voltage at the TAV zero crossing which is due to the change of the flatband potential between the passivated and bare samples. TAV vs V also has rather sharp peaks and valleys. Preliminary time constant measurements also show similar peaks and valleys at the proper applied voltages as shown in the figure. This behavior can be explained by postulating the presence of defect levels within

the bandgap. Another explanation might be due to the strong hysteresis effect which is also observed in the C-V curves of passivated samples. Thus the data might point to the fact that proper equilibrium was not reached in the measurement. However, further detailed measurements are needed before any definite conclusions can be drawn.

Fig. 7 shows the TAV-V data for CdTe. At zero bias it is positive and increases dramatically for positive bias. However, for negative bias, very little change is observed. Noting the shape of TAT vs carrier concentration in fig. 2(c), one can conjecture that the sample is p-type and tends to get inverted with positive voltage.

As discussed in ref. 2, from TAV-V plots using analytical modes and numerical computations, one can infer the flat-band potential and the equivalent interface charge density at the surface of the interface. However, this has not yet been performed.

In conclusion, the SAW nondestructive surface and interface characterization technique has been applied to CdTe and HgCdTe. The study shows that useful characterization is feasible although there is much to be performed before it becomes useful for production of devices such as focal plane arrays.

Acknowledgement

It is a pleasure to acknowledge the contribution of Dr. Peter Zimmermann of Honeywell Electro-Optics Division, through many discussions and sample preparations.

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TABLE I

	$Hg_{1-x}Cd_xTe$		CdTe
	T = [illegible]°K	T = 300°K	T = 300°K
Energy gap	0.46	0.433	1.56
Intrinsic carrier concentration	6×10^{15}	6×10^{14}	$\sim10^{7}$
Electron mobility	2×10^{5}	2×10^{5}	1000
Hole mobility	250	200	100
Dielectric constant	15	15	10.3

TABLE II

Sample #	$Hg_{1-x}Cd_xTe$	Passivation	N_A (cm^{-3})	Hole mobility ($cm^2/V\cdot sec$)
A	x = .4	No	$\sim$	200
B	x = .43	3500 Å Zinc Sulphide	$\sim 7.8\times10^{14}$	340
C	x = 1	No	2×10^{15}	100

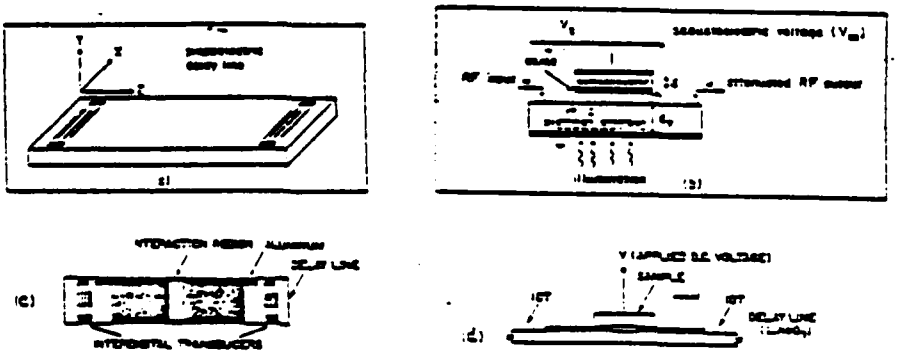
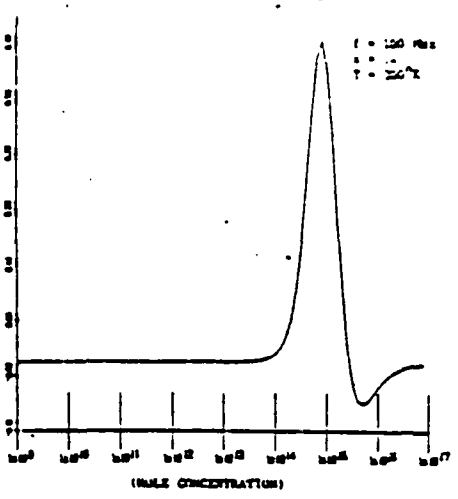
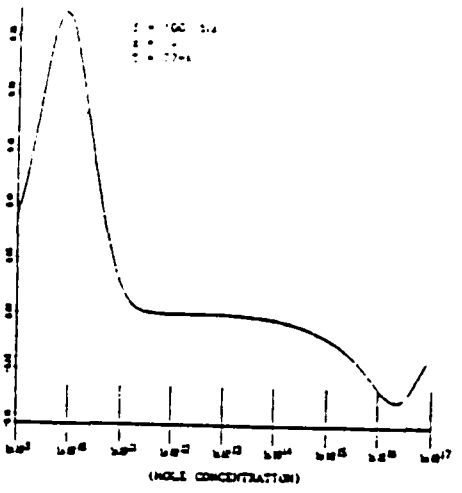


Fig. 1 Delay line structures used in TAV measurements

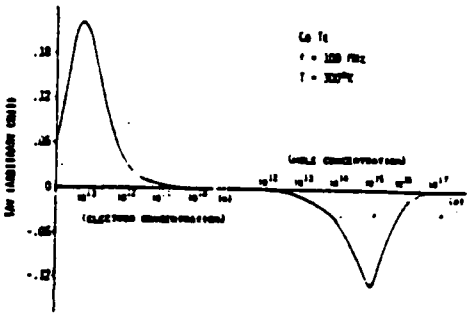


(a)

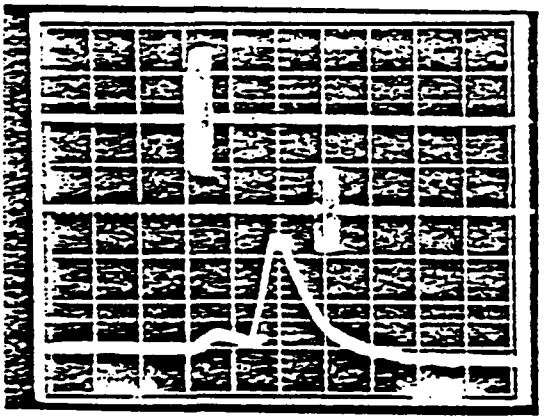


(b)

Fig. 2 Theoretical plot of TAV vs electron,hole concentration. a) $Hg_{1-x}Cd_xTe$ ($x = 0.4$) at 300°K, b) $Hg_{1-x}Cd_xTe$ ($x = 0.4$) at 77°K, c) CdTe at 300°K



(c)



(a)

(b)

(c)

Fig. 3 RF pulse input, output and TAV waveforms: Trace (a): Input RF pulse, frequency = 110 MHz, vertical scale = 5V/div., horizontal scale = 5 μsec/div., trace (b): output RF pulse, vertical scale = 0.5V/div., trace (c): TAV signal, vertical scale = 1 mV/div., horizontal scale = 5 μsec./div.

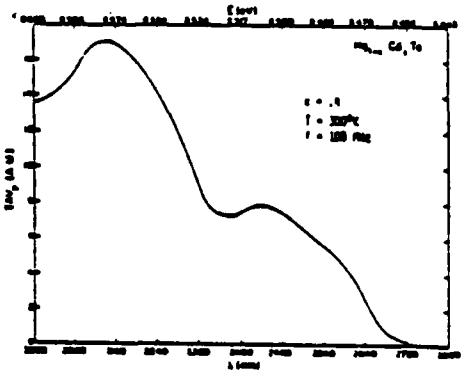


Fig. 4 TAV spectrum for Sample A

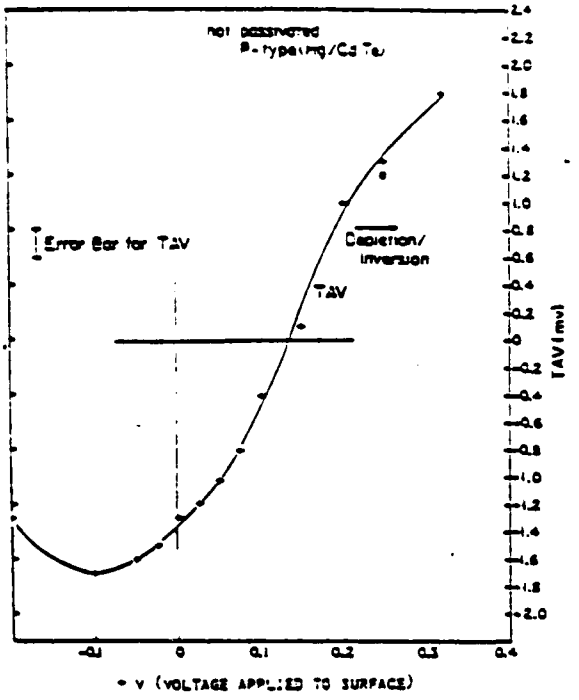


Fig. 5 TAV-V curve for $Hg_{.6}Cd_{.4}$ at T = 300°K, f = 100 MHz

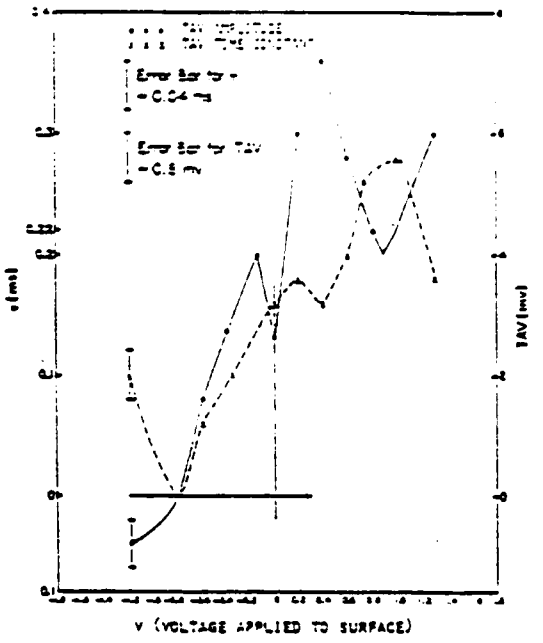


Fig. 6 TAV-V curve for $Hg_{.55}Cd_{.45}Te/ZnS$ at T = 300°K, f = 100 MHz

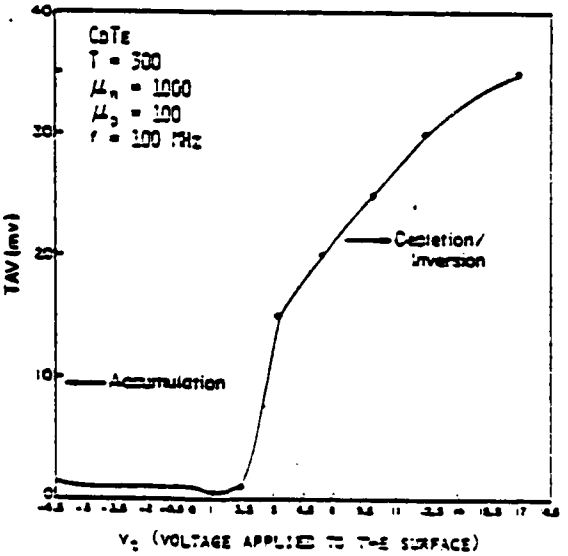


Fig. 7 TAV-V curve for CdTe at T = 300°K, f = 300 MHz

Spectroscopy of InAs using SAW generated transverse acoustoelectric voltage

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(Received 13 October 1978; accepted for publication 20 August 1979)

Transverse acoustoelectric voltage has been measured as a function of incident photon energy in an InAs on $LiNbO_3$ SAW delay line structure. A large transition at 1.5 eV is observed, which is confirmed by photocurrent measurement. Application of the large acoustoelectric voltage to image scanning and signal processing is presented.

PACS numbers: 72.50. + b

The interaction of a surface acoustic wave (SAW) with free carriers in a semiconductor medium separated from the piezoelectric surface has been studied by many authors in recent years.[1-5] This acoustoelectric effect or nonlinear interaction between semiconductor space charge carriers and SAW has been used in many real time signal processing applications. Nondestructive evaluation of electrical properties of semiconductor surfaces using the separated media convolver has also been performed.[6,7]

The SAW generated on a piezoelectric substrate is accompanied an electric field both inside and outside the crystal. The electric field penetrates the semiconductor sample placed on the $LiNbO_3$ crystal surface to the order of a Debye length. The acoustoelectric voltage produced by this nonlinear interaction has two components: one longitudinal in the direction of propagation and the other transverse, normal to the surface. This paper deals with the use of the transverse acoustoelectric voltage to study the electrical properties of InAs. The transverse acoustoelectric voltage (TAV) depends on the conductivity (σ) of the semiconductor, going to zero for $\sigma \to 0$ and for $\sigma \to \infty$. It attains a maximum value between the above limits. Also, the polarity of the transverse acoustoelectric voltage changes with the type of carriers. The surface conductivity of the semiconductor may change when light is incident on it. The acoustoelectric voltage provides a means of measuring these changes in the conductivity. Therefore, from the spectral response of the acoustoelectric voltage, one can obtain information about photoinduced carrier transitions in the semiconductor.

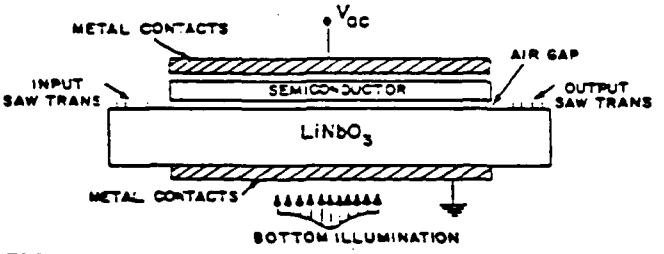

FIG. 1. Experimental configuration of SAW device for observing transverse acoustoelectric voltage.

Figure 1 shows a 100-MHz delay line structure with input and output SAW transducers spaced by a 10-μsec delay. The SAW is excited by five-finger-pair interdigital tran-

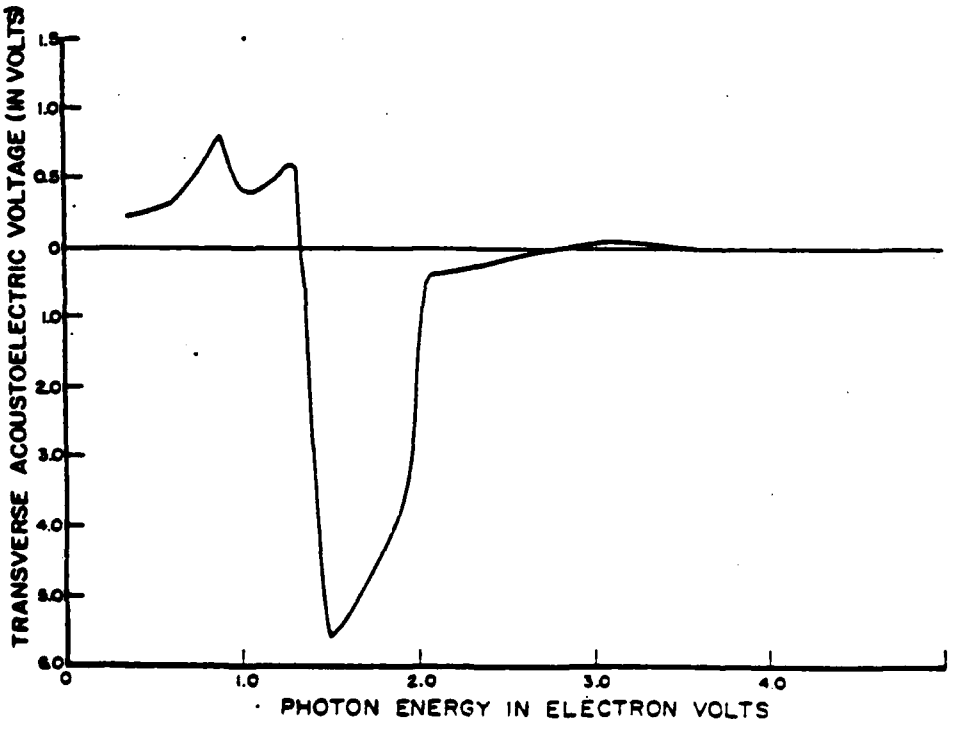

FIG. 2. Spectral response of the transverse acoustoelectric voltage for InAs. (Gain of 100 for positive values, gain of 1 for negative values).

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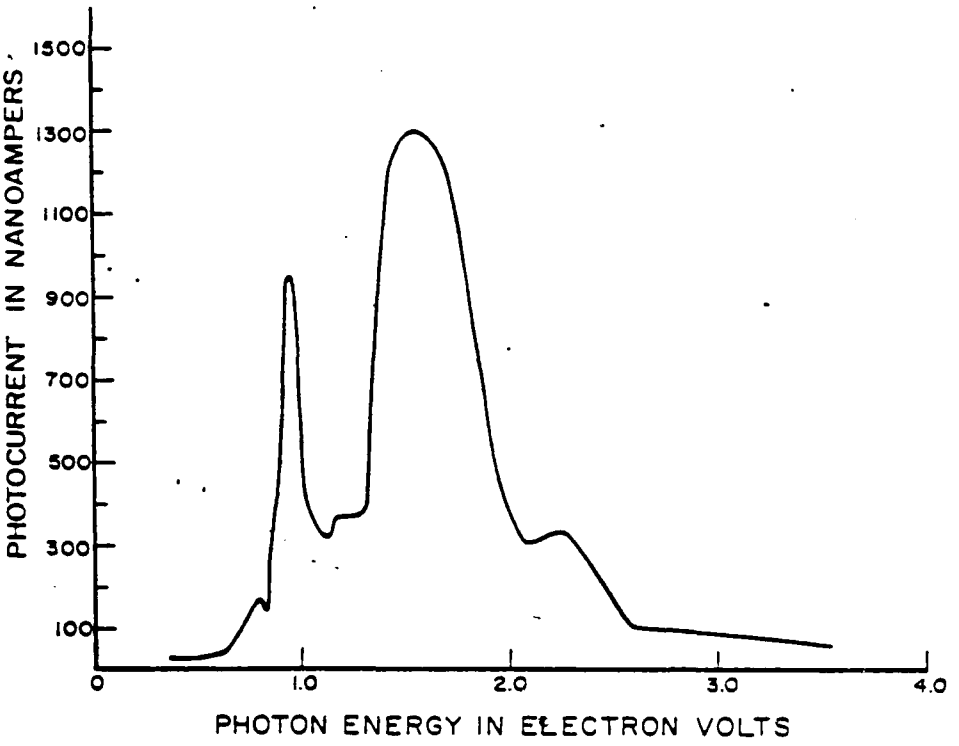

FIG. 3. Plot of surface photocurrent VERSUS photon energy.

ducers deposited on the surface of y-cut Z-propagating $LiNbO_3$. The semiconductor sample is placed above the delay line and carefully aligned to give a uniform gap between them. To measure the acoustoelectric voltage, three different contacts of (i) silver paint, (ii) aluminum foil, and (iii) indium were made on the top surface of the semiconductor. In all three cases, no significant difference was observed in the experimental results presented here. In the metal electrode deposited on the bottom surface of the $LiNbO_3$, a small slit is made to allow the light to fall on the semiconductor.

The semiconductor samples used were InAs epitaxial layers of n on n^+ with resistivity of about 1 Ω cm. The epitaxial layer was grown by the liquid phase epitaxy technique. The dimensions of the two InAs samples were 5×10 and 8×15 mm. One of the samples was etched and little difference was found between the experimental results obtained from the etched and nonetched samples. The semiconductor surface was uniformly illuminated from the bottom of the delay line through the slit using a Bausch and Lomb monochromator. Three gratings of ranges 0.3–0.8, 0.7–1.6, and 1.4–3.2 μm, respectively, were used. Appropriate filters were also used to eliminate the higher-order spectrum. A rectangular rf pulse of 5 msec duration and 12 V peak to peak was applied to the input of the SAW transducer. The acoustoelectric voltage was observed on an oscilloscope through a very high-impedance amplifier ($\sim 10^{12}\ \Omega$) with unity gain. The polarity of the acoustoelectric voltage in dark confirms that the InAs was n type.

Figure 2 shows the acoustoelectric voltage for different wavelengths of light illumination normalized to the radiant flux output of the monochromator. It is noted that there are three distinct peaks at 0.89, 1.33, and 1.495 eV. Because of the practical limitations the spectral response below and around the band gap of InAs could not be performed. The most important point in Fig. 2 is that there is a change in polarity of the voltage wave forms at 1.34 eV, followed by a large transition with a minimum at 1.495 eV. This agrees very well with the Hilsum[8] and Cardona[9] predictions about the indirect transition in InAs around 1.5 eV. The surprising result is the magnitude of the acoustoelectric voltage, which is of the order of 5.6 V. The maximum acoustoelectric voltage reported for Si and GaAs is very small, on the order of a few tens of millivolts. At 2.07 eV the slope drops and at 2.8 eV a transition occurs changing the sign of the acoustoelectric voltage from negative to positive. This may correspond to a higher energy transition of 2.85 eV.[10] The peak at 0.89 eV can be attributed to the transition from the lower valence band to the bottom of the conduction band, as it is known that the splitting of the InAs valence band due to spin-orbit coupling is approximately 0.44 eV and the band gap is known to be around 0.4 eV. The large acoustoelectric voltage can be attributed to the high mobility of InAs. The acoustoelectric current density is given by[11]

$$J_{ae} = \frac{-\mu I (2\alpha)}{v_s},$$

where α is the attenuation constant, μ is mobility, v_s is the SAW velocity, and I is the SAW input power per unit area. Since the mobility of InAs is of the order of 30 000 cm^2/V sec, one can expect a large acoustoelectric voltage. Though the mobility of InAs is 4 times greater than that of GaAs, the observed TAV is about 50 times greater. Therefore, this large anomaly in the TAV cannot be attributed solely to the large mobility. We are investigating other possibilities.

In order to verify the above results, surface photocurrent experiment was performed. Figure 3 shows the normal-

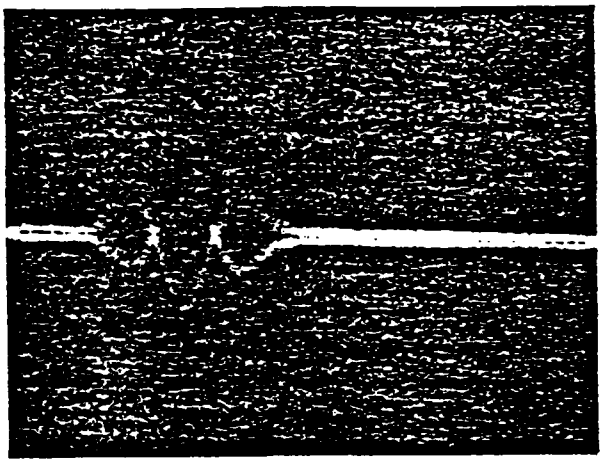

FIG. 4. Photograph of optical image scanning of the letter H. Fourier transforms of two slits.

ized photocurrent for different wavelengths of incident light. To measure the surface photocurrent, two metallic contacts using silver paint are used on the n surface of InAs. Between these leads, a dc power supply and a picroammeter are connected in series. The photocurrent generated by shining light is measured at a constant bias voltage. It is interesting to note that the position of the peaks occur around the same place as that of the acoustoelectric voltage.

To study the effect of temperature variation on the energy transition at 1.495 eV, we repeated the experiment at various temperatures, starting from 100 to 300 °K in steps of 50 °K. The variation of the energy transition with above temperatures shows drooping characteristics varying from 1.65 to 1.49 eV.

The large acoustoelectric voltage observed at 1.5 eV provides potential applications of the gap coupled semiconductor piezoelectric device such as an optical image scanner[12] or as a convolver.[1]

For optical image scanning, the longitudinal acoustoelectric voltage produced by the nonlinear interaction of free carriers in a semiconductor and SAW were used. The optical pattern incident on the semiconductor surface changes its conductivity, resulting in the modulation of the acoustoelectric voltage. Since the ratio of the acoustoelectric signal with light to the signal without light is very large, a high-contrast ratio is obtained. The scanning along the vertical direction is

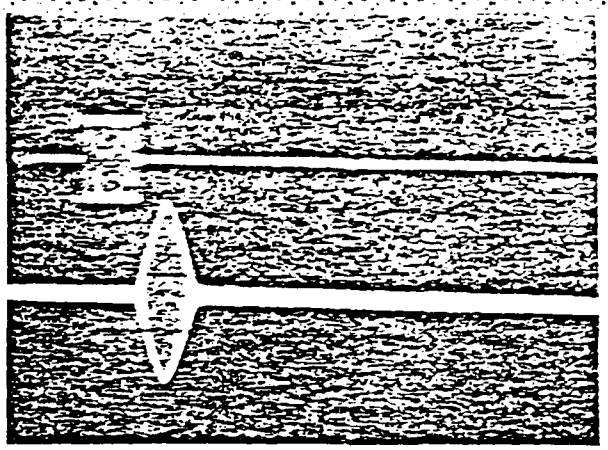

FIG. 5. Autoconvolution of one rf pulse (horizontal scale 1 μsec/div, vertical scale 20 mV/div).

performed mechanically. The most important factor which characterizes any image scanner is its resolution. The resolution of this image scanner depends upon the pulse width of the SAW. Figure 4(a) shows the oscilloscope display of the image of the letter H. In this, the acoustoelectric signal was directly applied to the z axis of the oscilloscope without a preamplifier. Figure 4(b) shows the Fourier transform of two slits obtained by exciting either side of the SAW delay line with an rf chirp signal.

The autoconvolution of one rf pulse with light incident on the semiconductor is shown in Fig. 5. It is well known that a large dc TAV indicates large convolved output. The performance of any convolver can be described[13] by the figure of merit, (M),

$$M = V_{oc} W (P_{s1} P_{s2})^{1/2}, \tag{2}$$

where V_{oc} is the steady-state rms open-circuit voltage, W is the acoustic beam width, and P_{s1} and P_{s2} are the input acoustic powers. The experimental value of M for this convolver is 7.5×10^{-2} Vm/W, which is large compared to the results so far obtained using other semiconductors. The only disadvantage of this convolver is that light must be present at all times. The measured peak convolved output with normalized light intensity of different wavelength gives exactly the same peaks as those of Fig. 3.

In conclusion, from the spectroscopy of InAs above the band gap and from the photocurrent and transverse acoustoelectric measurements, we have shown that a very large transition occurs around 1.5 eV, which agrees with the published results. The observed large acoustoelectric voltage has been successfully used to perform optical image scanning and real-time signal processing. However, why such anomalously large TAV is obtained in InAs cannot be explained.

ACKNOWLEDGMENTS

The authors wish to thank Dr. K.P. Pande, Dr. J. Borrego, Mr. R.T. Webster, Mr. H. Estrada-Vazques, and Miss Bhavana Baxi for useful discussion. This work is partially supported by Air Force Office of Scientific Research Grant No. 77-3426 and Office of Naval Research Contract No. N00014-75-C-0772.

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Studies on CdS*

To study the surface state characteristics of the semiconductor at the presence of the electrolyte, a thin layer of electrolyte is introduced between the semiconductor and the piezoelectric material (Figure 3.13). When the surface wave reaches the electrolyte, layer waves are generated in the electrolyte. If the semiconductor is also piezoelectric, as in the CdS, a large TAV is developed. The TAV measurements are performed on CdS samples with the electrolyte consisting of 0.1N solution of $NiCl_2$. The role of aqueous solution of $NiCl_2$ is to induce a depletion layer in the CdS surface, both for resembling the real solar cell conditions and also to increase the TAV measurement sensitivity by lowering the conductivity of the surface. The depleting effect of the aqueous solution of $NiCl_2$ is tested by measuring the open circuit voltage of a cell consisting of CdS and 0.1N $NiCl_2$ which is negative (-0.8V). The spectral response of TAV is obtained by recording the TAV peak while shining monochromatic light on the sample. In most of the experiments, two beam spectroscopy is used. In this method a bias light with constant intensity and wavelength shines on the sample while another light with constant intensity but varying wavelength illuminates the sample

*This is taken from Mr. B. Davari's Master's Thesis.

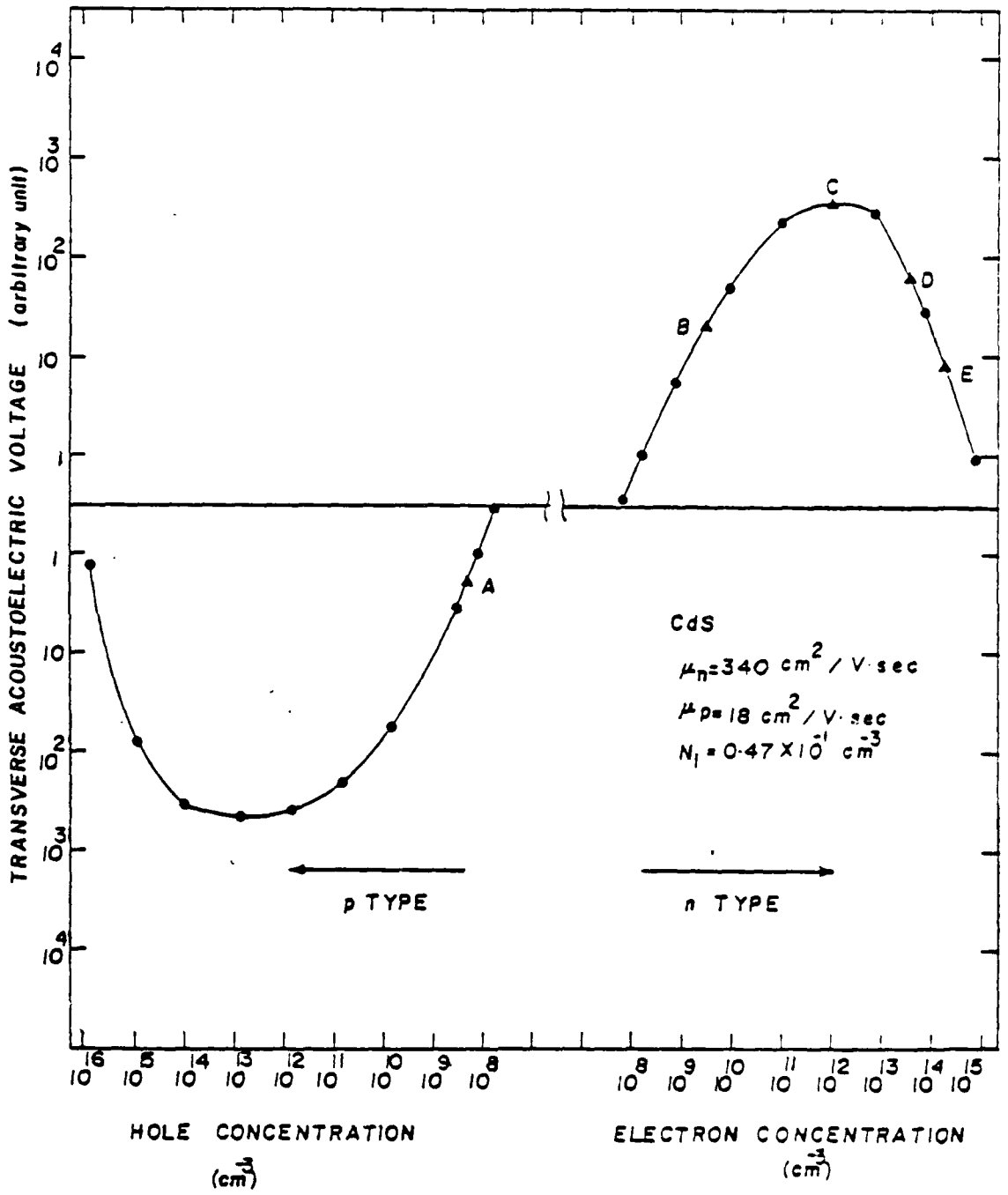

Figure 3.12 TAV Amplitude as a Function of Carrier Concentration in CdS

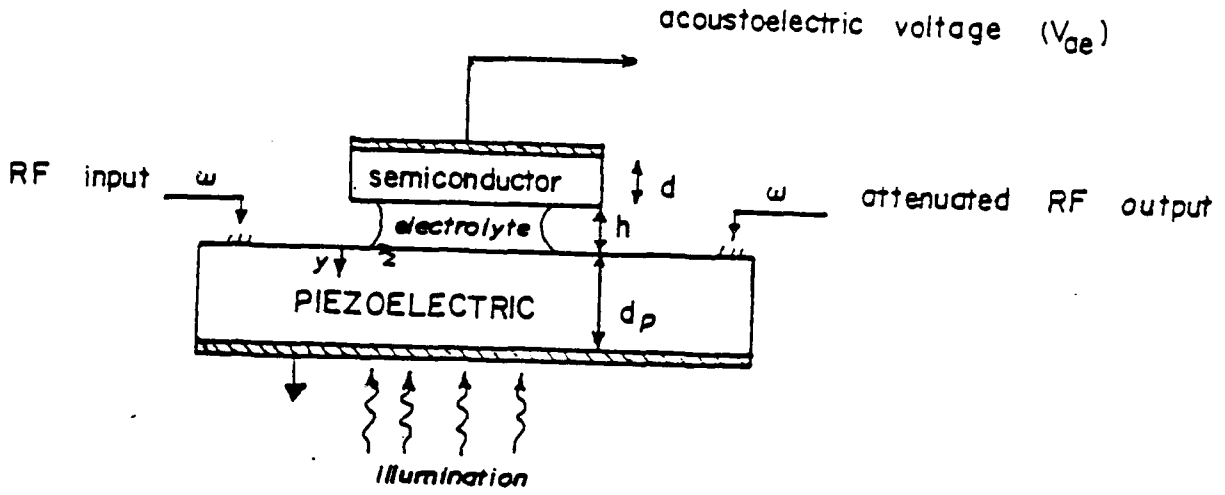

Figure 3.13 Configuration Used for Semiconductor Electrolyte Interface Study Using SAW Technique

simultaneously. The transverse acoustoelectric voltage (TAV) spectral response is obtained to determine the position of the surface states energy levels in CdS samples worked under short circuit condition in a SLJ cell. In the one beam spectrum shown in Figure 3.14, the TAV for the long wavelengths is very low corresponding to low conductivity. Going toward shorter wavelengths, there is a broad minimum around 900 nm where the TAV is negative, indicating a strong contribution from holes (It should be noted that the sample is n type in the dark). This part of the curve corresponds to the region around the point A in Figure 3.12. For shorter wavelengths the TAV polarity changes from negative to positive and the amplitude increases as the conductivity increases (around point B in Figure 3.12). At about 640 nm the TAV reaches a maximum corresponding to the point C in Figure 3.12. The conductivity increases more for wavelengths shorter than 640 nm which causes the TAV to decrease (point D in Figure 3.12). At 520 nm which is the bandgap of CdS the conductivity is maximum and TAV is at the relative minimum (point E in Figure 3.12). For wavelengths shorter than 520 nm the TAV increases indicating the lower conductivities (moving towards point C in Figure 3.12).

To explain the minimum around 900 nm some interface levels should be considered in the CdS bandgap. More detailed structure of the interface levels can be found using two beam spectroscopy [9,27]. Figure 3.15 shows the TAV spectral response using a bias light supplied by a mercury lamp. In this curve in addition to a minimum around 900 nm there is another broad minimum around 1500 nm. To

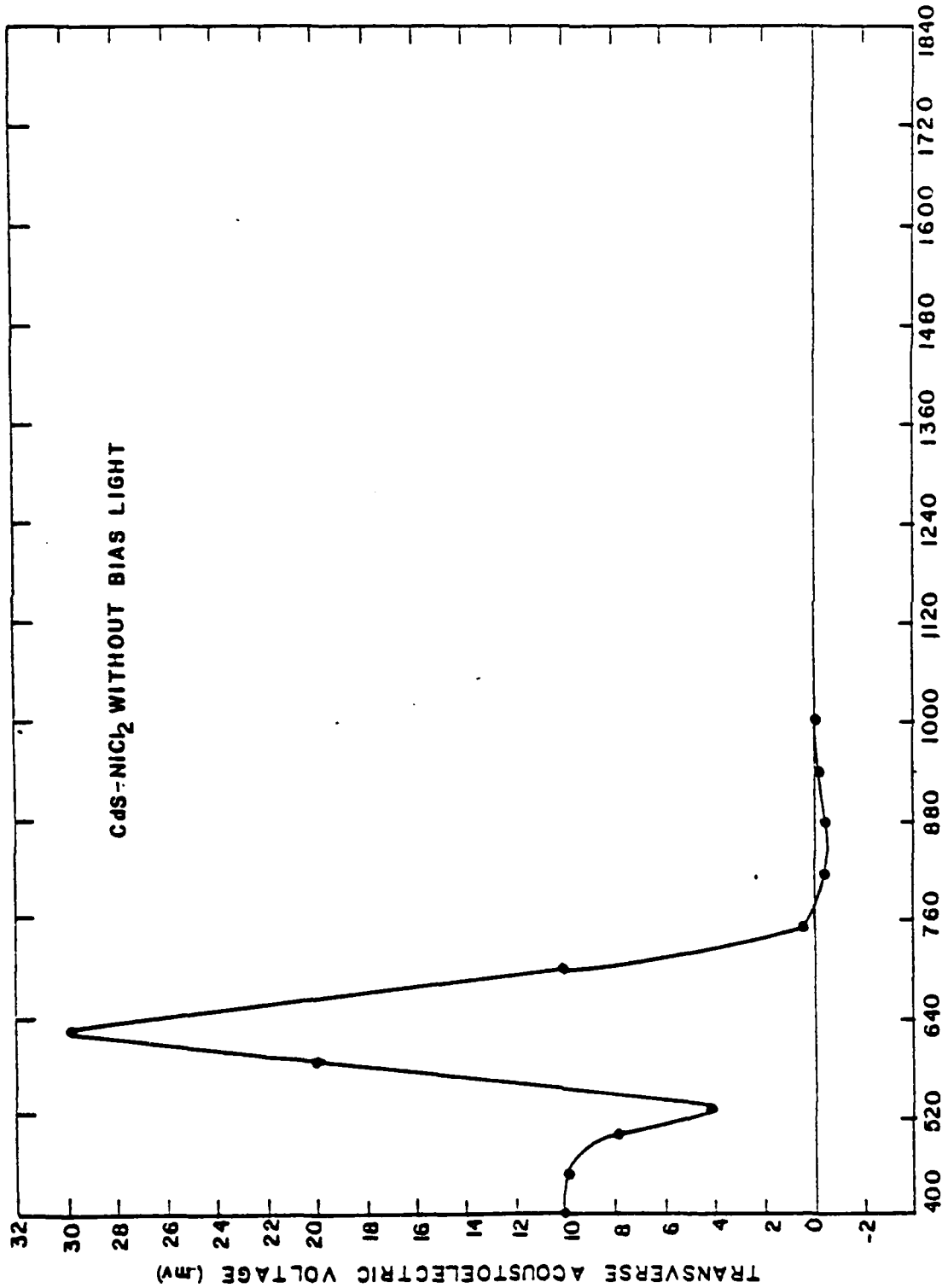

Figure 3.14 One Beam TAV Spectral Response for CdS-$NiCl_2$ System

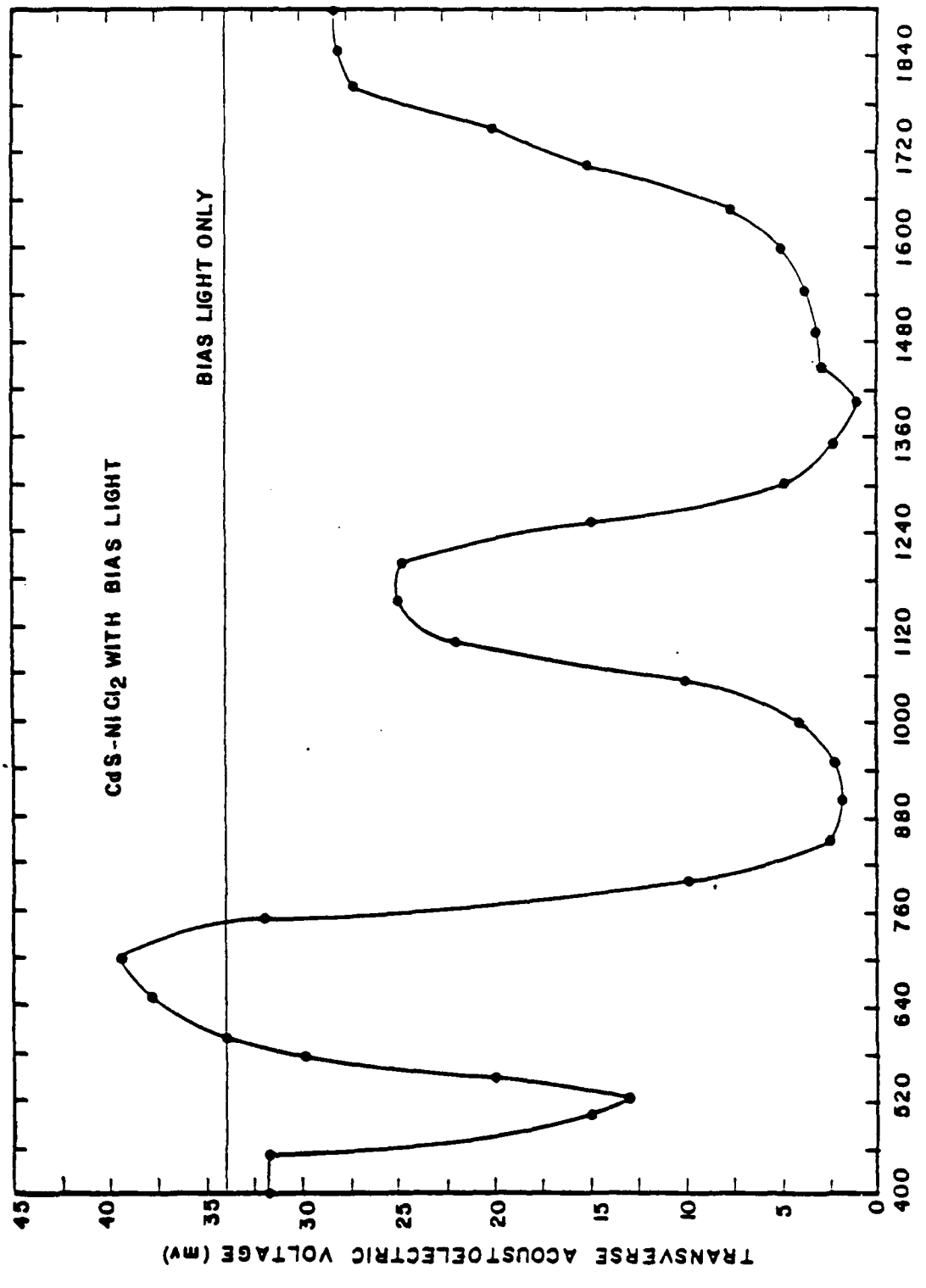

Figure 3.15 Two Beam TAV Spectral Response With Bias Light From a Mercury Arc Source

explain the mechanism that can be responsible for this spectral response, consider the band diagram shown in Figure 3.16. The conduction and valance bands are shown along with the Fermi level and two dashed lines representing the interface levels which are assumed to be acceptor levels. In the presence of the bias light, the levels are empty. When monochromatic light of the proper energy strikes the semiconductor, electrons make a transition from the valence band to the interface level leaving a hole behind and pulling the quasi Fermi level down. Since the contribution of the holes to the TAV is negative the TAV is lowered. To confirm the band diagram shown in Figure 3.16, spectroscopy using a monochromatic bias light was performed. Using 500 nm as the bias light the result is shown in Figure 3.17. As one might expect the two minima around 900 nm and 1500 nm can be seen, indicating that the bias light has excited both the interface levels. For longer wavelengths up to 750 nm (corresponding to the excitation energy of the level Ea_2 in Figure 3.16) both minima should be seen. The spectral response for 750 nm bias light is shown in Figure 3.18. Bias light with energy between the excitation energy of the levels Ea_2 and Ea_1 should show only one minimum. No minimum should be seen for bias wavelengths greater than 1090 nm (the excitation energy of the level Ea_1 in Figure 3.16). Using 1090 nm bias light the electrons from the Ea_1 level should be excited and a minimum around 900 nm should be observed. In fact only a very slight effect from this level can be seen (Figure 3.19). This may be due to the fact that the level is

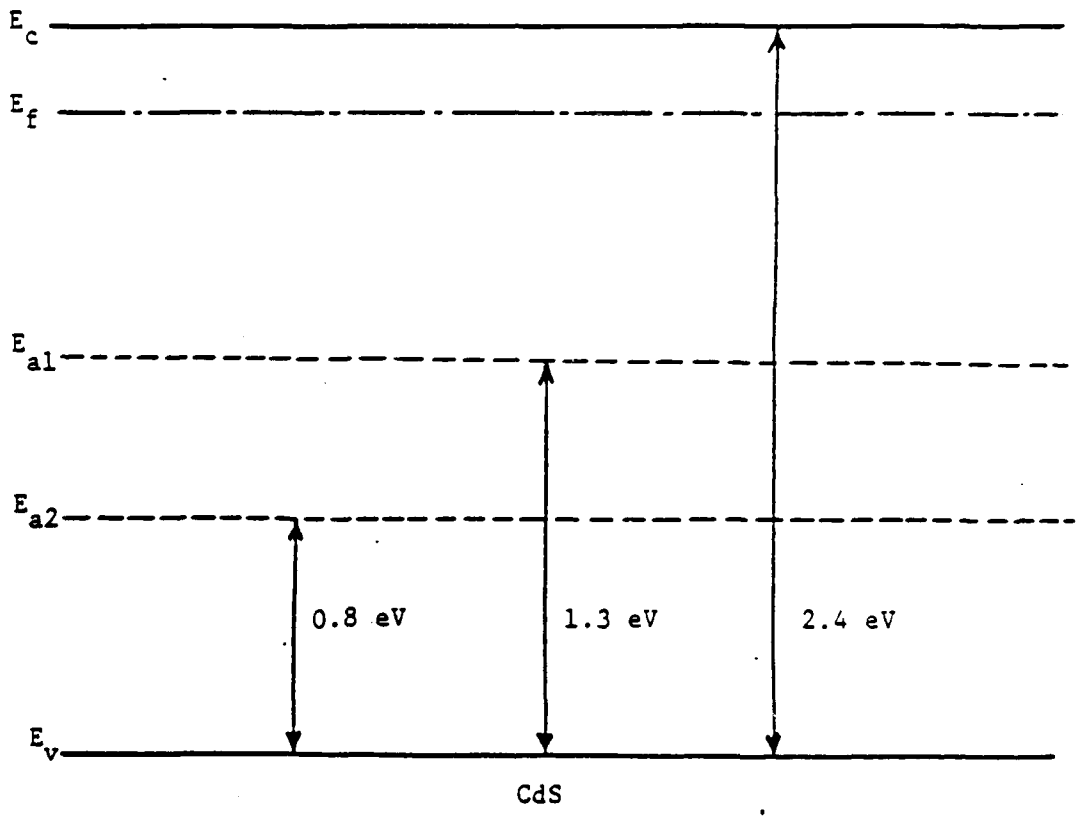

Figure 3.16 Energy Band Diagram for CdS, Showing the Position of the Acceptor Interface States

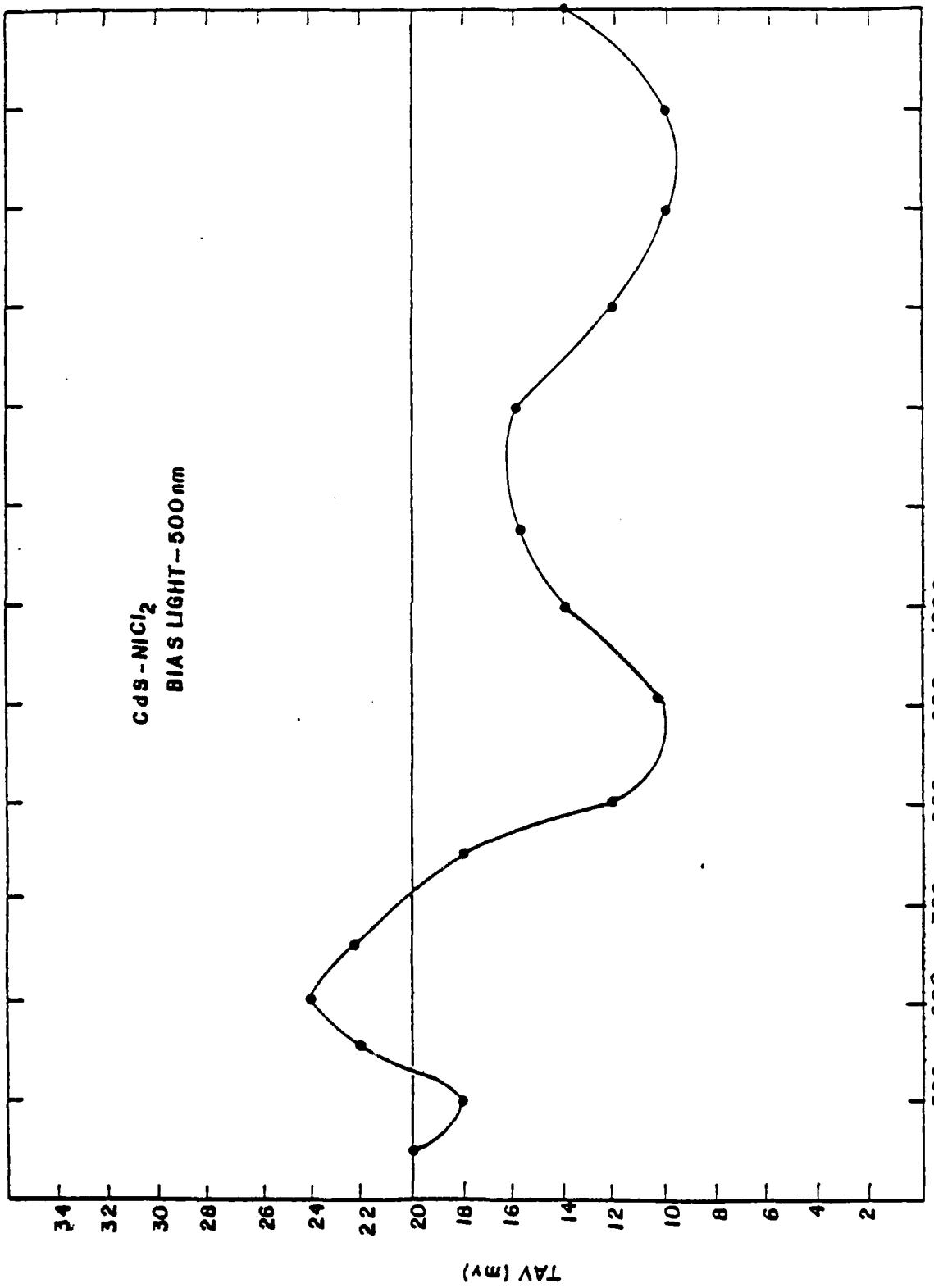

Figure 3.17 Two Beam TAV Spectral Response Using 500 nm Bias Light

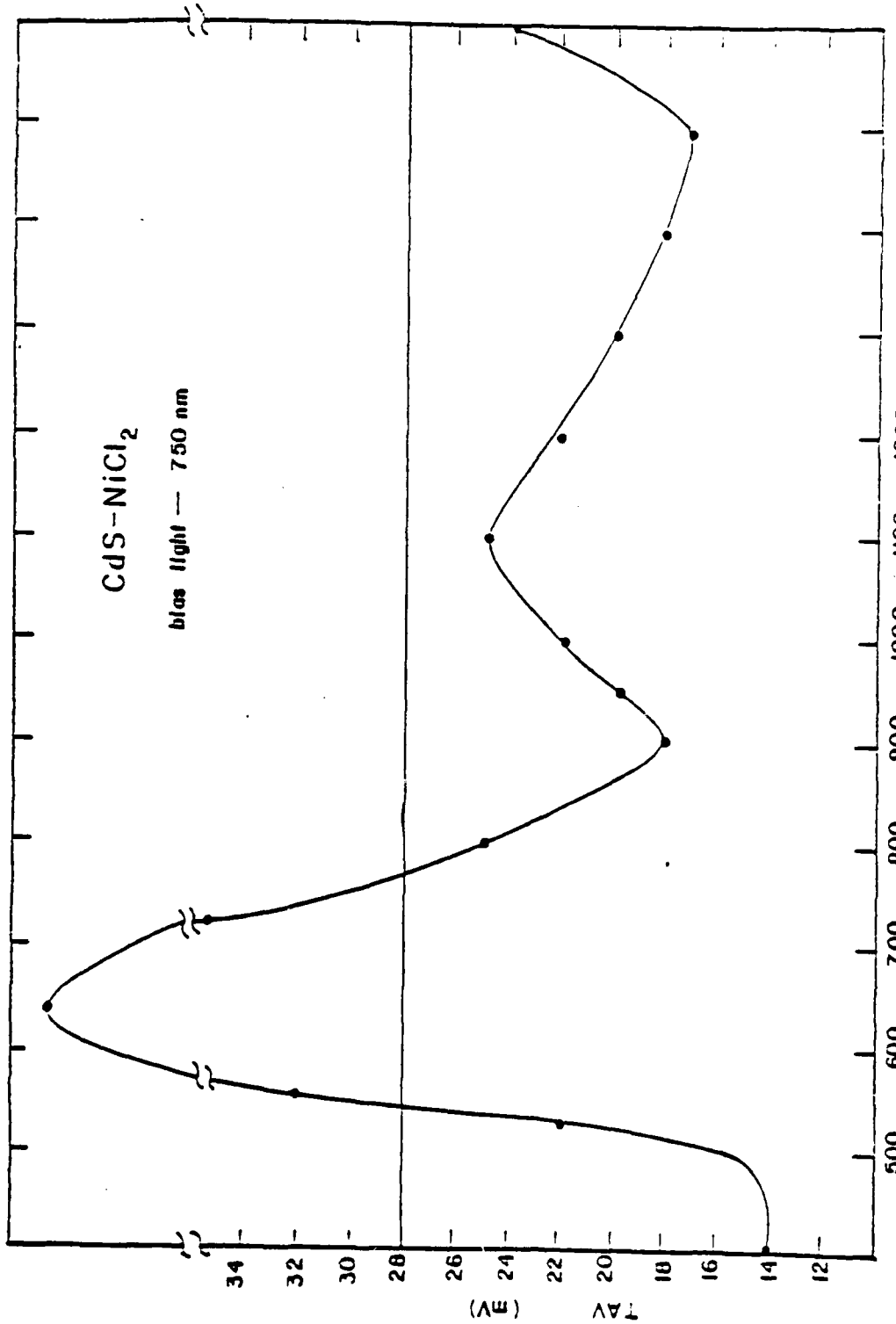

Figure 3.18 Two Beam TAV Spectral Response Using 750 nm Bias Light

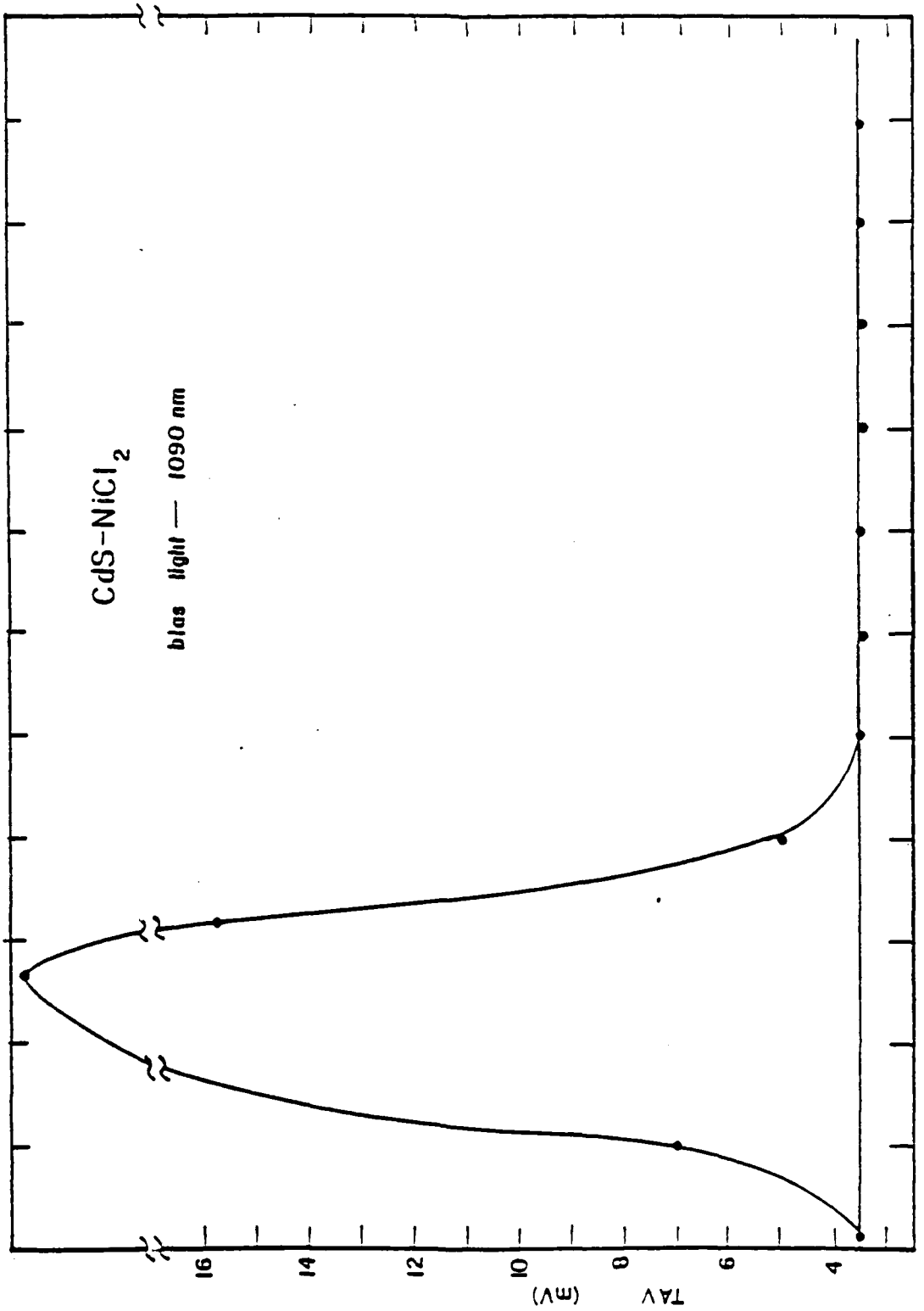

Figure 3.19 Two Beam TAV Spectral Response Using 1090 nm Bias Light

near the center of the gap. Since the passband of the monochromator is fairly large, there may be a transition of electrons from the valance band to the level and then from that level to the conduction band, so the net result would not have a strong effect on the Tav [27].

In summary, two broad minima, one around 920 nm and one around 1500 nm, are observed in the TAV spectral response. We believe these are caused by two bands of electron acceptor levels, one centered at an energy of 0.8 eV above the valance band and the other at 1.3 eV above the valance band. The advantage of this technique is that except for one contact at the back of the semiconductor, there is no need for any other contact to measure the surface characteristic of the semiconductor.

The second technique, used to detect the interface states which is suitable for high conductivity samples if the photoconductivity spectroscopy. In this method a small DC voltage (2 volts) is applied to both ends of the CdS slabs by two silver epoxy contacts and the surface phtooconductivity of the sample is monitored by measuring the current passing through the circuit. The sample is again illuminated with one or two monochromatic radiation. Using the photoconductivity two beam spectroscopy, the presence and the position of the interface states can also be detected. The result of photocurrent spectral response is shown in Figure 3.20. It can be seen that again two broad minima around 900 and 1400 nm are present in the two beam spectrum. Using the same argument as for

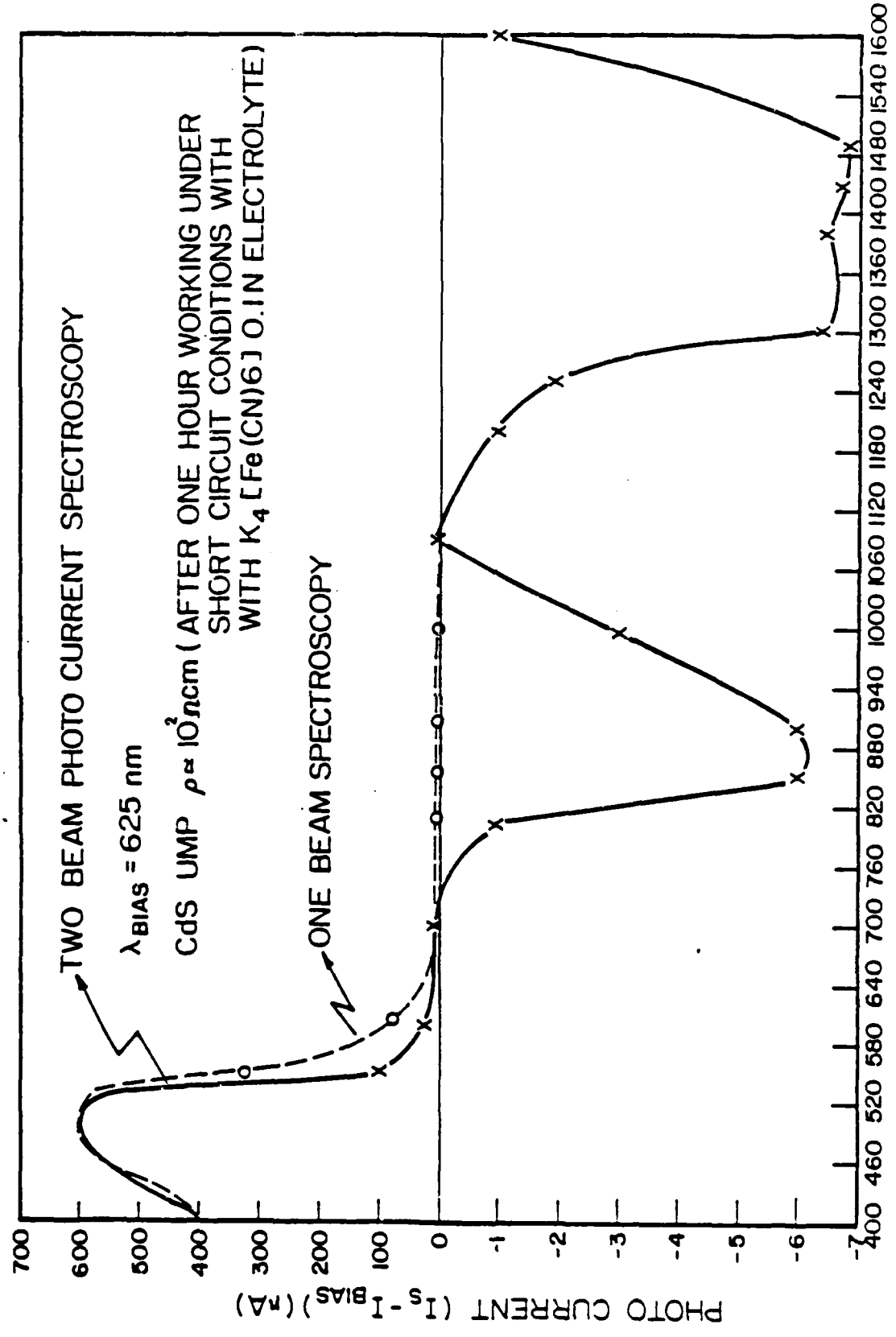

Figure 3.20 Two Beam Photo Conductivity Spectroscopy Using 625 nm Bias Light

the TAV spectral response, the two acceptor level bands are assumed to be responsible for this structure. It should be noted that using only the scan beam (one beam condition in Figure 3.20) does not reveal the effect of the surface states. It should also be considered that the y axis of this plot is the value of photocurrent produced by the variable wavelength (scanning) beam, minus the photocurrent generated by the bias light [9,27].

3.5 Junction Capacitance-Voltage (C-V) Measurement to Obtain the Experimental Flatband Potential (E_{fb}) for the CdS/$[Fe(CN)_6]^{4-/3-}$ System and the CdS Free Carrier Concentration. Determination of the Cell Complete Band Diagram Measured by the Above Techniques (Including the Interface States [22]

The C-V measurements are performed on the CdS/$[Fe(CN)_6]^{4-/3-}$ cell at dark condition. On the positive voltage scan (CdS with respect to Au counter electrode) the semiconductor surface is depleted. If most of the applied voltage is dropped across the CdS space charge region rather than the electrolyte double layer, then the $1/C^2$ versus voltage will be a straight line [8]. The plot of the $1/C^2$ versus voltage is shown in Figure 3.21. The value of flatband potential can be determined from the x intercept of the curve and it is about -0.6V. Also the straight line passing through the data points, indicates that indeed most of the voltage drop is across the CdS space charge. The free carrier concentration is determined from the slope of the C^{-2}-V curve, using the following equation.

$$\frac{dC^{-2}}{dV} = \frac{2}{q\,\varepsilon_s\varepsilon_o\,N_D} \qquad (3.9)$$

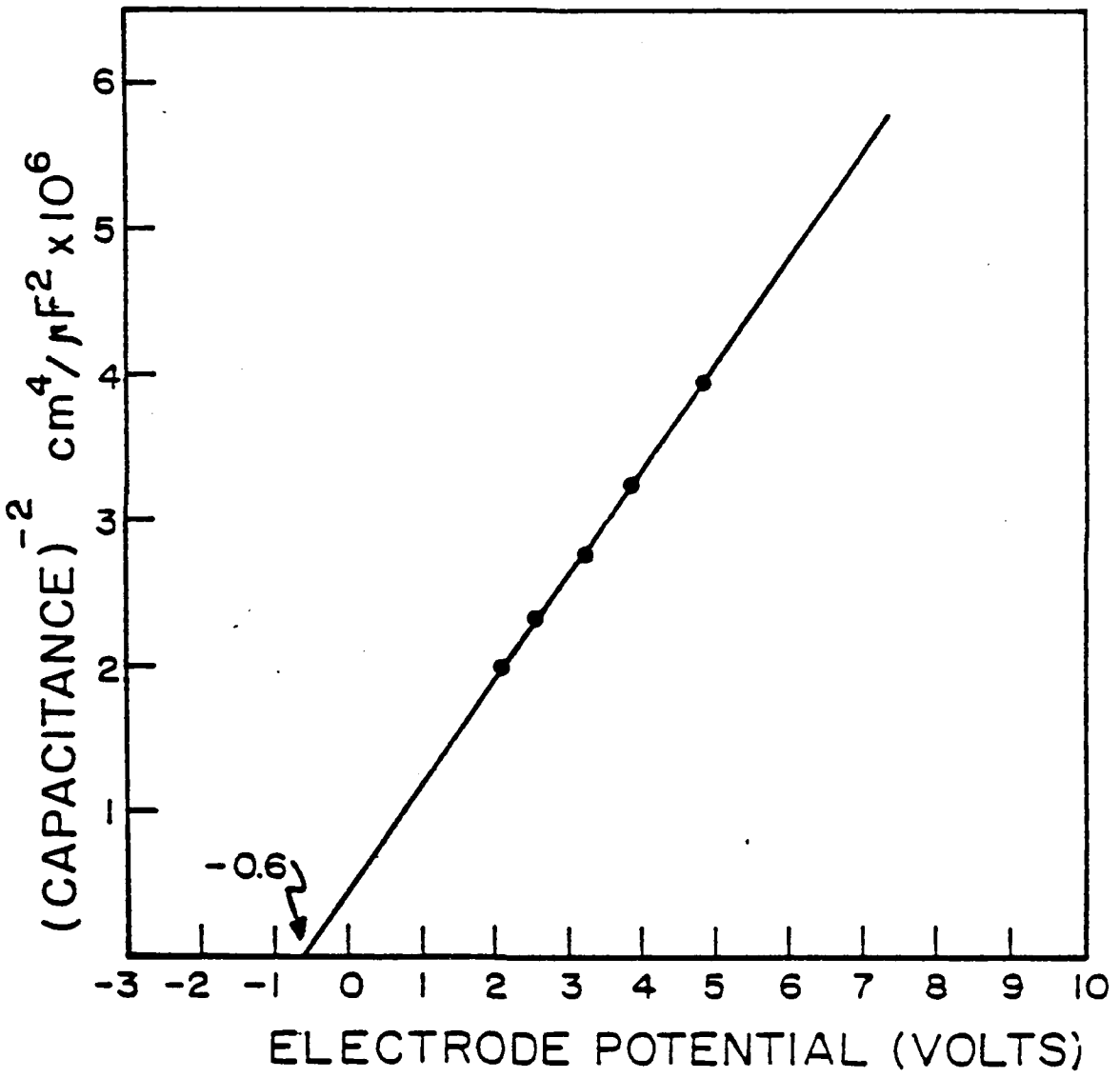

Figure 3.21 C^{-2} Curve Versus the Potential of CdS with Respect to Au for CdS-$K_4[Fe(CN)_6]$ System (Dark)

where: C is the capacitance per unit area (F/cm^2), V is the voltage (volts), q is the electronic charge, ε_s is the CdS relative permitivity (≈ 10), ε_o is the free space permitivity (8.86×10^{-14} F/cm) and N_D is the doping concentration (cm^{-3}). From the slope of the plot in Figure 3.21 the carrier concentration of about 2×10^{13} cm^{-3} can be estimated. Using the value of about 0.5×10^{-1} cm^{-3} for intrinsic carrier concentration (n_i), the Fermi level energy can be calculated. The position of Fermi level is approximately 0.3 eV below the conduction band. This value was used before (Section 3.1) in order to construct the equilibrium band diagrma. Knowing the flat band potential and the position of Fermi level, the experimentally measured band diagram of the CdS/$[Fe(CN)_6]^{4-13-}$ system is obtained. This band diagram is shown in Figure 3.22 along with the decomposition potential (E_D^o). The energy levels of the two acceptor levels, detected by the techniques discussed in the previous section are also indicated. The comparison of the band diagram presented in Figure 3.22 with the theoretically calculated band diagram (Figure 3.2b) (where the effect of interface states in adjusting the flat band potential is neglected) shows that indeed the pinning of Fermi levels via surface states is not a dominant factor in determining the flat band potential.

3.6 Two Beam Short Circuit Current Spectroscopy to Determine the Effect of Interface States on the Solar Cell Short Circuit Current [22]

The relative positions of the redox Fermi level E_{fr} and anodic decomposition Fermi level E_D^o (Figure 3.22) shows that the

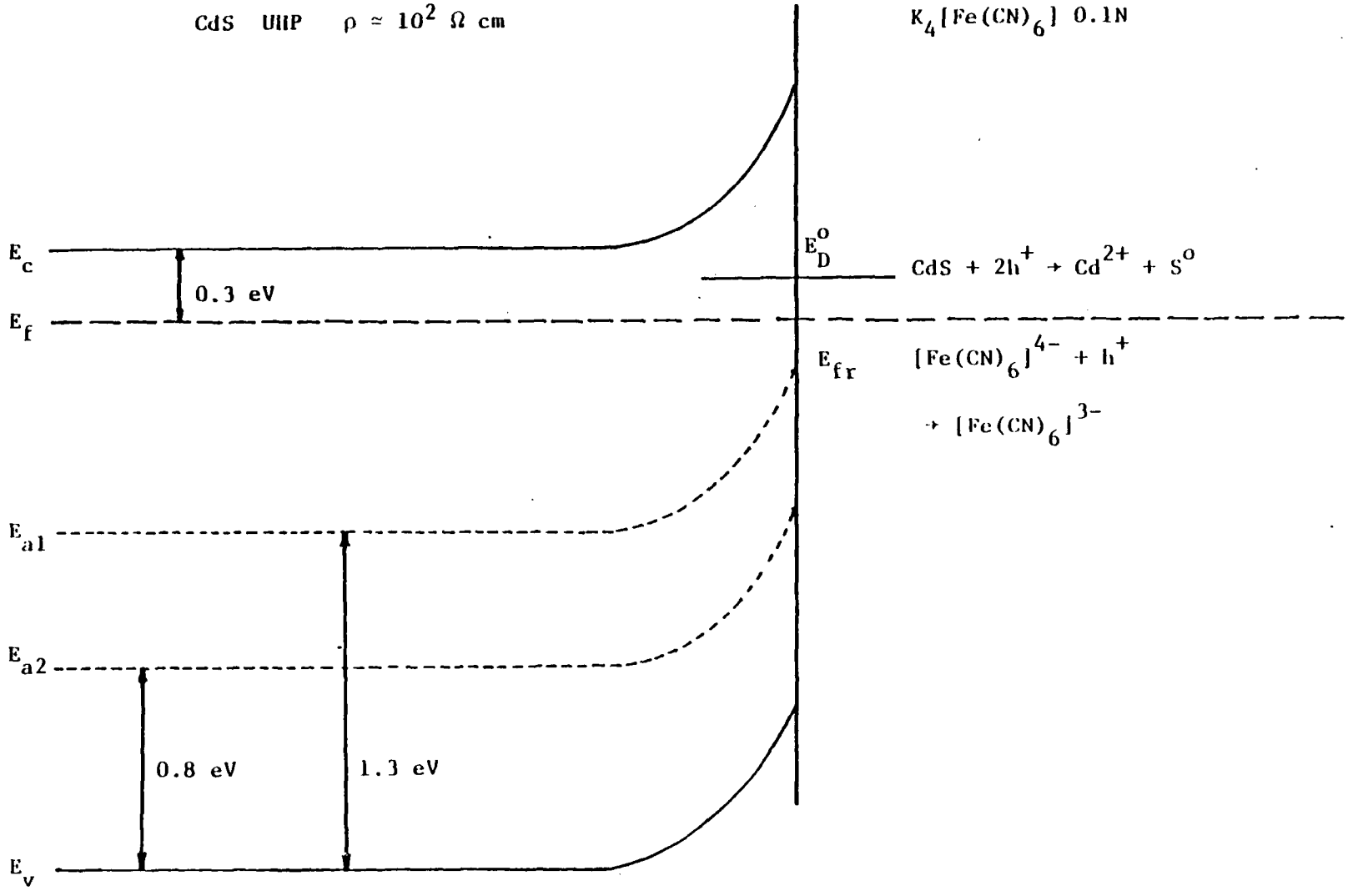

Figure 3.22 Energy Band Diagram for CdS-$K_4[Fe(CN)_6]$ System

competition between the redox charge transfer and anodic decomposition is possible (also discussed in Section 2.2.4 and 3.2). Surface states can affect the redox charge transfer rate by providing a current path for photogenerated holes from the valence band to the filled states of the redox electrolyte (Section 2.2.5). This effect can be observed by the two beam short circuit current spectroscopy of the CdS/$[Fe(CN)_6]^{4-/3-}$ cell shown in Figure 3.23. The short circuit current generated by the bias light (λ = 520 nm, intensity ≈ 10 $\mu w/cm^2$) is shown as the straight line. The quenching of the short circuit current below the bias light value can be observed for scanning wavelengths below 800 nm with minima around 900 and 1400 nm. The minima can be associated with the energy level differences between the valence band and the acceptor levels (Figure 3.22). Thus the excitation of electrons from the valence band to the acceptor levels by incident beams at 900 nm (1.3 eV) and 1400 nm (0.8 eV) reduces the short circuit current. This effect is much more pronounced (about two orders of magnitude) for the cells constructed with high resistivity CdS ($\rho \approx 10^4$ Ωcm) samples.

Short circuit current quenching can be due to the following reasons. First, the excitation of electrons from the valence band to acceptor levels partially fills these levels and the charge transfer of photogenerated holes from the valance band to the redox levels via these acceptor levels is appreciably reduced. Second, the conductivity of CdS decreases upon illumination with wavelengths of about 900 and 1400 nm. Thus the IR drop in the cell increases,

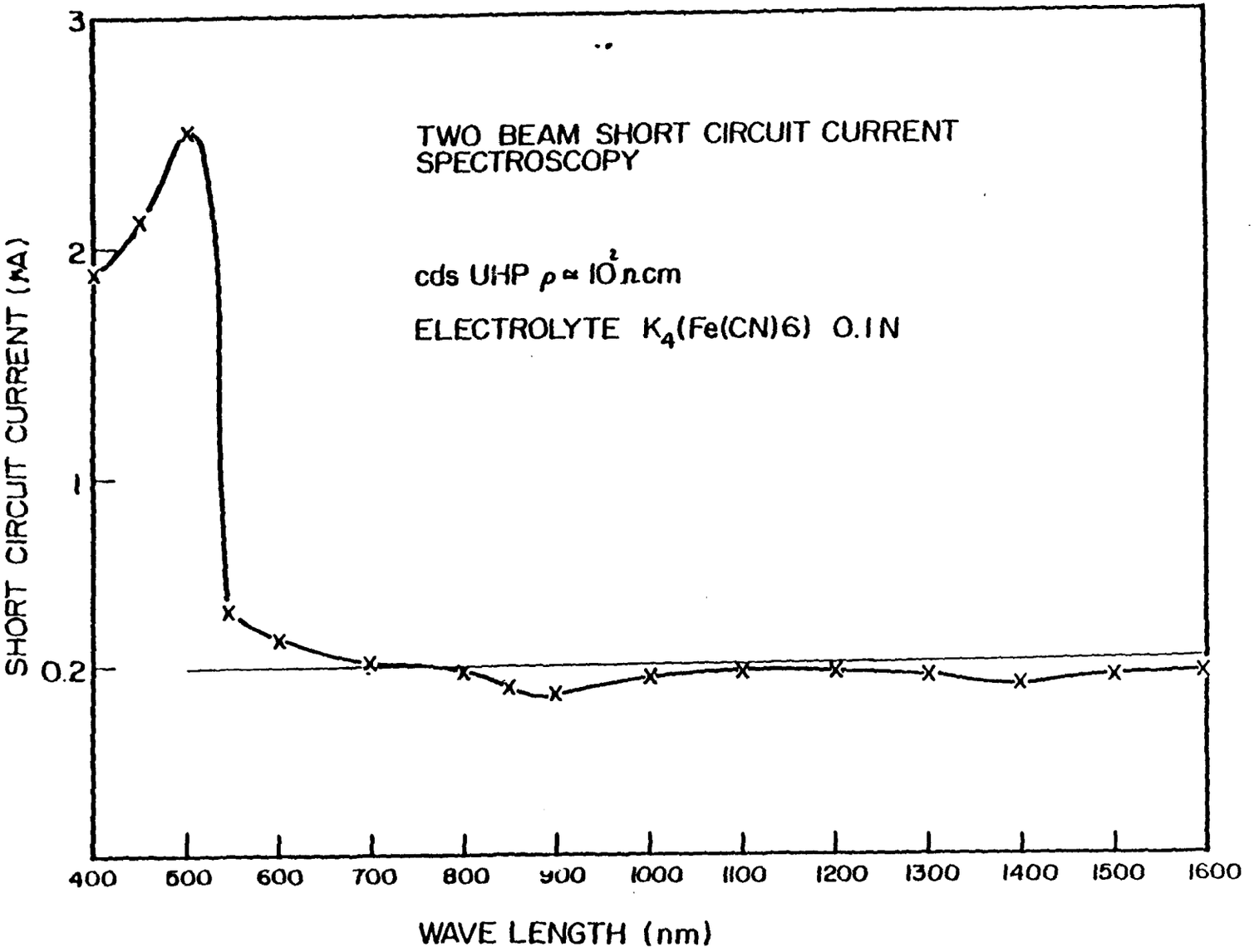

Figure 3.23 Two Beam Short Circuit Current Spectroscopy for the CdS-$K_4[Fe(CN)_6$ System (λ Bias < 750 nm)

causing the reduction of short circuit current. It should be noted that although surface states increase the redox charge transfer rate, they can also aid the anodic decomposition by transferring photogenerated holes form the valence band to the decomposition energy level (E_D^o in Figure 3.22).

CHAPTER 7

CONCLUSION

Properties of semiconductor surfaces and interfaces play a vital role on the electrical characteristics of the devices fabricated on semiconductor surfaces. Considering today's rapid advancements in the area of planar fabrication processes used in VIHISIC and VLSI chips, the effect of surfaces on device performance is of increasing importance. This report encompasses both the theoretical and experimental aspects of the research related to the characterization of silicon and compound semiconductors (such as gallium arsenide, cadmium sulfide) surfaces and interfaces.

The major emphasis of this report is on a new and novel surface acoustic wave (SAW) device which has been developed under this grant for use in the nondestructive determination of the electronic properties of semiconductors. The technique uses surface acoustic waves on a piezoelectric substrate. The electric field associated with the SAW interacts with free carriers of a semiconductor placed near the piezoelectric surface. The interaction generates detectable currents in the semiconductor and attenuates the SAW. By observing these effects while varying external parameters such as temperature, applied acoustic power, SAW frequency, semiconductor surface irradiation and bias voltage, the desired information is obtained. The properties that can be determined by this non contact technique include the bulk and surface conductivity, generation lifetime, surface recombination velocity, the location in the energy gap of traps, surface states, and interface states, trap emission and absorption times and storage times in the depletion layer. The technique can be used to perform depth profiling of electrical properties. Because the properties are measured without any contact and the measurement is localized to a

small region of the wafer, one can envision an automated equipment, using this SAW technique, where 256x256 points (for an example) on the wafer can be evaluated with respect to lifetime and surface generation velocity. The results can be shown in the form of images in pseudocolor where each color represents a certain range of the parameters.

The SAW characterization of the semiconductor could be performed at progressive stages of device fabrication thereby improving yield by identifying faulty processing steps. Thus, the implementation of the new and more conventional, already existing techniques (such as C-V, C-t, SEM, voltammetry, etc.) reveal the critical semiconductor surface and interface properties before and after the semiconductor has undergone a specific processing step, e.g., thermal oxidation, etching, polishing, annealing (Si) and anodic oxidation (GaAs). A brief listing of the research performed towards the application of this technique in determining different electrical properties of different semiconductors follows:

* Silicon: The nondestructive SAW technique is greatly improved by the introduction of a new delay line structure which has enabled us to vary the surface potential via a small external DC bias field (about 100 times smaller than the previous work and comparable to C-V technique) while the transverse acoustoelectric voltage (TAV) amplitude and transient time constants are measured. TAV amplitude is a function of the near surface electron and hole conductivity difference and the TAV transient time constants can be approximately related to the carriers generation lifetime (τ_g) and the surface generation velocity (S_g). Parameters such as oxide charge, flat-band voltage, generation lifetime and surface generation velocity can be determined at different surface potentials. The above parameters are evaluated to characterize the following: thermally grown oxides, the

effectiveness of the back surface laser induced damage (LID) gettering on the reduction of the defect density on the device side of the wafer and the effects of chemical etching, polishing and forming gas annealing on the carrier lifetime. The feasibility of the nondestructive depth profiling of the free carrier concentration and some of the above parameters are demonstrated by the introduction of a new profiling procedure and its application to ion implanted silicon wafers. In summary the possibility of the TAV measurement under a small DC bias field (comparable to C-V) while utilizing a nondestructive configuration has dramatically enhanced the applicability of this technique for quantitative measurements. Transient capacitance (C-t), capacitance voltage (C-V) and spreading resistance measurements are also used for the characterization of silicon wafers and in some cases the results are compared with the TAV amplitude versus voltage (TAV-V) and TAV transient time constant measurements.

* GaAs: Two beam TAV spectroscopy is applied in order to reveal the subbandgap energy level structures. In two beam spectroscopy the wavelength of one beam is fixed (bias light) while the wavelength of the second beam (secondary light) is scanned in the desired range. The presented data on the subbandgap interface states which are either due to the intrinsic nature of the surface discontinuity or due to the interface with anodically grown oxide indicate the following: 1) The presence of a high density acceptor level at about 1 eV above the valence band and the increase of the density of these states by anodic oxidation, 2) The effect of the different oxidation schemes on the density of interface states, leading to an optimum oxidation current versus time waveform. This waveform consists of low oxidation current density ($J \simeq 0.1$ mA/cm^2) in the nucleation and

island coalescence phase (for a better GaAs/oxide interface) followed by a rapid continuous oxide growth phase ($J \simeq 0.5$ mA/cm^2) in order to ensure a good oxide bulk quality ($\sigma < 10^{15}$ Ωcm, breakdown field $> 5.5 \times 10^6$ V/cm), 3) Detection of the characteristic exciton peak at low temperatures and the quenching of this peak by 1 eV bias light which is attributed to the increase of the hole density by electron transition from valence band to the high density acceptor level, 4) Detection of a band of donor levels at about 1.3 eV below the conduction band which is observable only at low temperatures or after oxidation. In GaAs and GaAs/oxide characterization, both the TAV and capacitance voltage (C-V) measurements are used for high and low resistivity materials respectively. The reason is the much higher sensitivity of the TAV technique at lower carrier concentration as opposed to the C-V technique.

* <u>CdS, InP, InAs (HgCd) Te</u>: In addition to the two beam TAV spectroscopy for the subbandgap energy level studies, the following investigations are conducted regarding the above semiconductors: 1) CdS is used as the working electrode in a semiconductor liquid junction solar cell configuration. A technique similar to cyclic voltammetry is applied to study the competition between redox charge transfer and the anodic dissolution of CdS in order to achieve a more stable cell configuration. Different parameters affecting the cell efficiency such as the counter electrode material and the tunneling through the thin insulator layer, produced by photo anodization are investigated. 2) Low temperature one and two beam TAV spectroscopy are performed on high resistivity Fe doped InP samples and the results demonstrate the characteristic exciton peaks and no quenching effect by bias light (as opposed to GaAs samples) which is attributed to a lower density of interface states. 3) TAV versus

voltage measurements are performed on (HgCd) Te samples to reveal the surface condition at zero bias (depletion, inversion) and possibly the magnitude of the interface charges.

CHAPTER 8

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APPENDIX A

I. Papers Published on the Subject of Non-Destructive Testing of Surface Acoustic Wave

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PATENTS

1. U.S. Patent No. 4,380,864, "Method for providing in-situ nondestructive monitoring of semiconductors during laser annealing process."

2. "Selective Anodic oxidation of semiconductors for pattern generation", to be filed.